Transient Simulations of GaAs MESFETs on Semi-insulating Substrates Compensated by Deep Levels

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GaAs MESFETs are now important devices for high-speed and high-frequency LSIs. GaAs MESFETs are fabricated on the semi-insulating substrate compensated by deep levels, and hence the MESFET characteristics strongly depend on junction properties between the active layer and the substrate. However, most of the numerical models have neglected this impurity compensation. Proposing a model including this effect, we have studied DC characteristics and small-signal parameters of GaAs MESFETs[1]-[3]. In this work, we have made transient simulations of GaAs MESFETs on the substrate with deep levels, and have found a unique feature originated from existence of deep levels.

The device structure simulated here is shown in Fig.1. As a substrate, we consider undoped semi-insulating LEC GaAs where deep donors "EL2" (N_{EL2}) compensate shallow acceptors (N_{Ai}). Basic equations are 1)Poisson's equation including the ionized deep-donor term, 2)rate equation for the deep donor, 3)continuity equations for electrons and holes, and 4)current equations for electrons and holes. These are solved numerically in two dimension.

Fig.2 shows responses of drain currents for 0.3 μm gate-length GaAs MESFETs when the drain voltage V_D steps from 0 V to 1 V. At $t \sim 10^{-11}$sec, the drain currents become constant temporarily (we call this "quasi-steady state"), but they decrease gradually during $t = 10^{-5}$ sec to 10^{-1} sec, reaching steady-state values. The changes of drain currents during this period are larger for higher acceptor and trap densities in the substrate. It is interpreted that "quasi-steady state" is a state where the deep levels do not response and electrons move under the same ionized-impurity densities as those for $V_D = 0$ V in this case. When the deep levels begin to capture electrons and the density of negative charges in the substrate becomes high to modulate the potential there (Fig.3), the channel thickness is reduced and the drain current begins to decrease. Fig.4 shows responses of drain currents for 0.3 μm gate-length GaAs MESFETs when V_D steps from 1 V to 0.5 V. Again, "quasi-steady state" appears during $t = 10^{-11}$ sec to 10^{-3} sec, then the drain currents begins to increase, reaching steady-state values. This increase in drain currents starts when the deep levels begin to emit electrons to widen the channel thickness.

Fig.5 shows an example of drain characteristics of GaAs MESFETs. The solid lines are steady-state curves. The dashed lines and the dotted-and-dashed lines are calculated under fixed ionized-impurity densities for $V_D = 0$ V and 1 V, respectively. (x) and (o) are values for "quasi-steady state" mentioned above, and agree well with the dashed lines and the dotted-and-dashed lines, respectively. These ascertain the interpretation that "quasi-steady state" is a state where the deep levels do not response. From Fig.5, we can say that I-V curves are dependent on how fast the voltage is sweeped and that hysteresis in I-V curves due to deep levels may be observed.

In conclusion, we have shown that in drain step responses for GaAs MESFETs, there exists "quasi-steady state" where deep levels do not response. I-V curves are quite different between this state and the steady state. Deep levels in the semi-insulating substrate are important factors to determine the characteristics of GaAs MESFETs.

[1] K.Horio et al., IEEE Trans. Electron Devices, 35, 1778 (1988).
[2] K.Horio and Y.Fuseya et al., IEEE Trans. Microwave Theory Tech., 37, 1371 (1989).
[3] K.Horio and Y.Fuseya et al., The 3rd Asia-Pasific Microwave Conference Proceedings, 963 (1990).

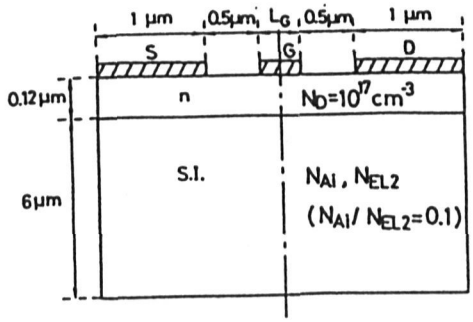

Fig.1 Device structure simulated in this study.

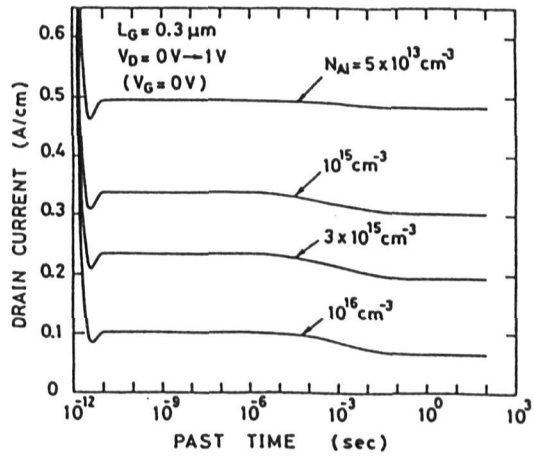

Fig.2 Responses of drain currents for 0.3 μm gate-length GaAs MESFETs when V_D steps from 0 V to 1 V.

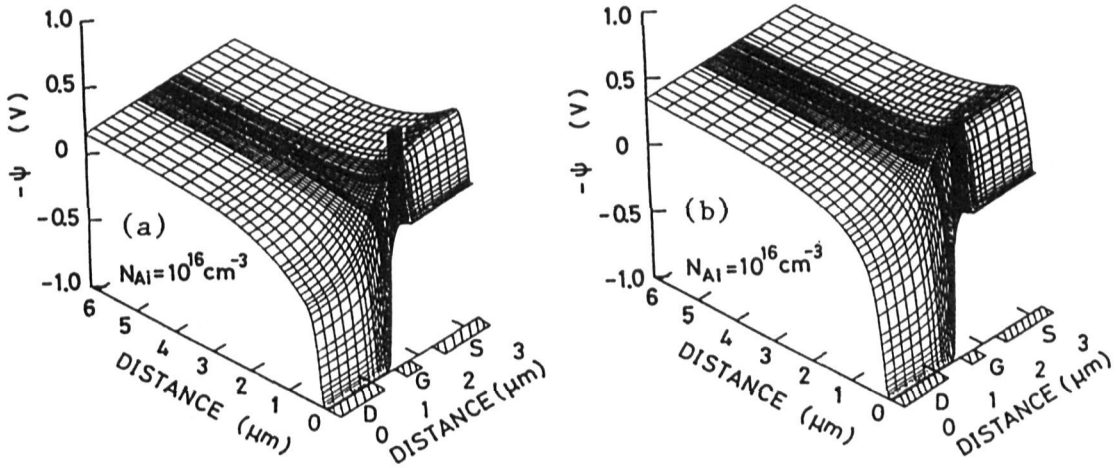

Fig.3 Potential profiles of 0.3 μm gate-length GaAs MESFETs when V_D steps from 0 V to 1 V. (a) t = 10^{-5} sec, (b) t = 10^{0} sec.

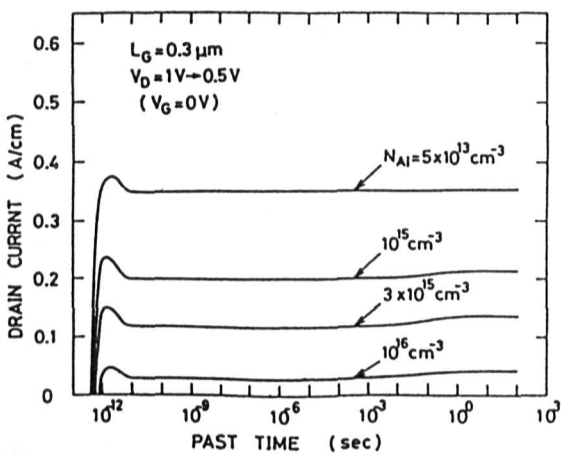

Fig.4 Responses of drain currents for 0.3 μm gate-length GaAs MESFETs when V_D steps from 1 V to 0.5 V.

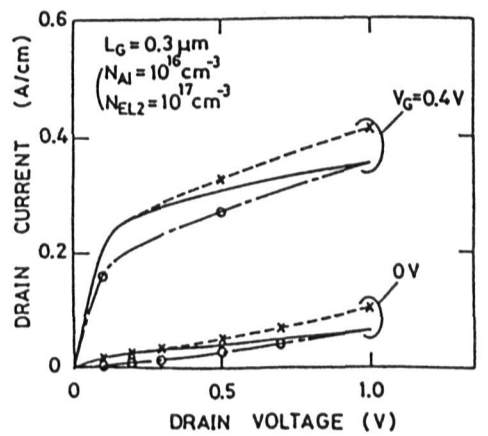

Fig.5 Drain characteristics of GaAs MESFETs.
(——): Steady state.
(– – –): Ionized impurity fixed (V_D = 0 V).
(—·—): Ionized impurity fixed (V_D = 1 V).
(x,o): Quasi-steady state.