AN ACCURATE CAD-ORIENTED ANALYTICAL MODEL FOR SHORT-CHANNEL MOS TRANSISTOR CAPACITANCES

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SUMMARY

The accuracy of the analytical device models used in circuit simulators plays a key role in the design and verification of integrated circuit performances. In particular, an accurate modeling of charges and capacitances in MOS transistors is extremely crucial for the simulation of VLSI circuits, expecially for dynamic RAMs, switched-capacitor and analog circuits. Recently, this aspect has been focused in detail and several analytical models have been developed to predict the behavior of the MOSFET intrinsic capacitances. However, even if the models presented in the literature makes it possible to obtain excellent results for long-channel devices[1], they are not accurate enough for short-channel devices because 2-dimensional effects have not yet been satisfactorily modeled[2,3]. In fact, the strong approximating hypotheses introduced in the set of fundamental semiconductor equations to get analytical models for the charges and capacitances behaviour of small-size devices reveal to be inadequate.
Purpose of this work is to present an accurate CAD-oriented model for the total capacitance coefficients of MOS transistors (i.e. including overlap and junction capacitances) valid for both long and short-channel devices. The model was derived on the basis of a new methodology recently presented which, once given a condition on the maximum acceptable error, has been proven [4] to be able to produce very accurate analytical models for VLSI MOSFETs and BJTs.
First of all a complete caracterization of the small signal operation of the MOSFET was performed with the aid of the two-dimensional simulator HFIELDS [5]. In particular, data were obtained for a wide range of channel length L and bias voltages (V_{GS}, V_{DS} and V_{BS}) values.
The methodology starts from a very simple zero-order capacitance model containing only a few parameters. Then a set of orthogonal continuous functions, satisfying the given condition on the maximum error, is derived by a fitting procedure applied to the data obtained from the simulator. Finally, a procedure able to introduce some new parameters which enable to achieve a more complex model which is a continuous function of all bias voltages and device parameters and still respecting the given condition on the maximum acceptable error, is implemented.
Figs 1-6 show some comparisons between the capacitance behaviour achieved with the model so obtained (continuous line) and the data obtained from HFIELDS (dots), for the most important independent capacitance coefficients. Figs.1 and 3 refer to a long-channel device with L=10μm, while figs.2 and 4 show results for a short-channel device with an effective channel length L=0.7 μm. In addition, the C_{gs},C_{gd} versus V_{gs} and the C_{dg},C_{gd} versus V_{ds} behaviours for different channel lengths values are reported in figs.5 and 6, respectively . As can be seen, the agreement between model and simulation is reasonably good. Finally, as an indicator of the achieved fitting, the normalized mean (percentage) error with respect to numerical simulations [5] is reported in Table I for devices with several channel lengths.

REFERENCES

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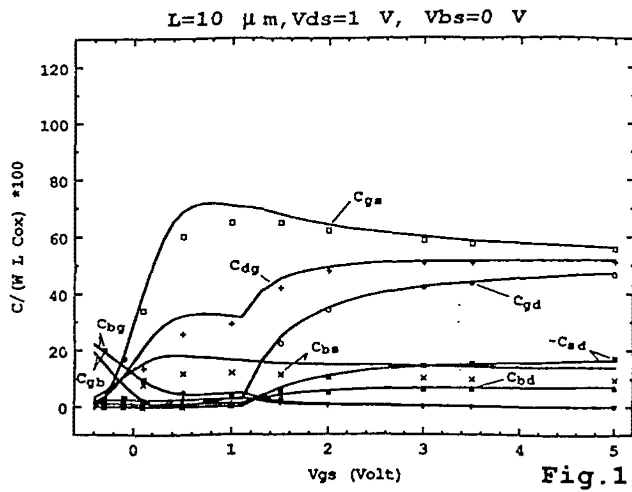

Fig.1

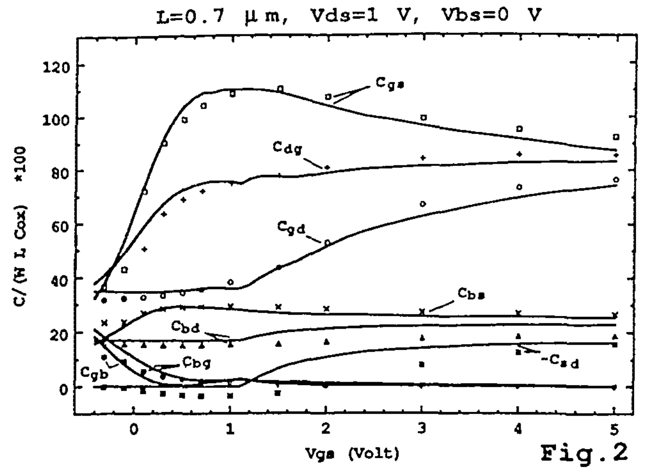

Fig.2

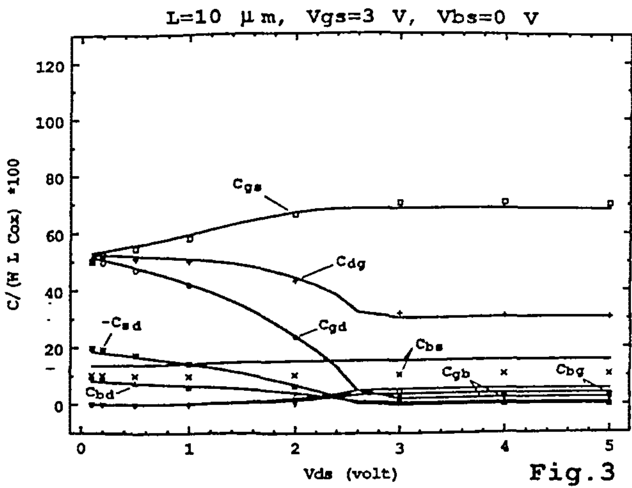

Fig.3

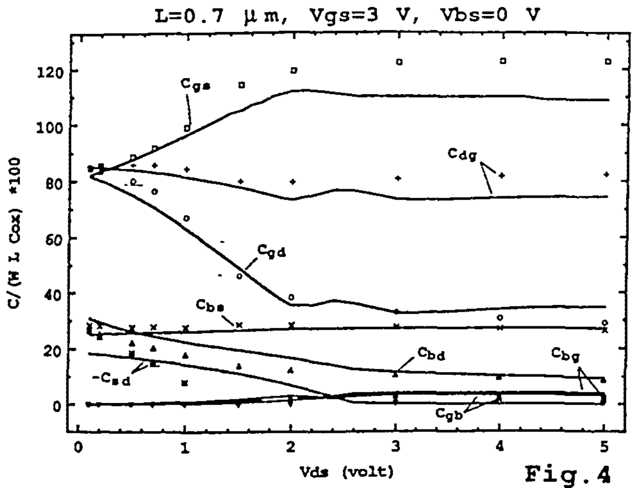

Fig.4

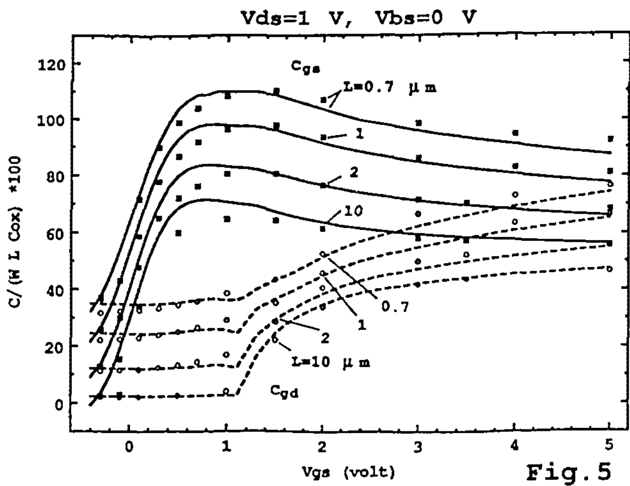

Fig.5

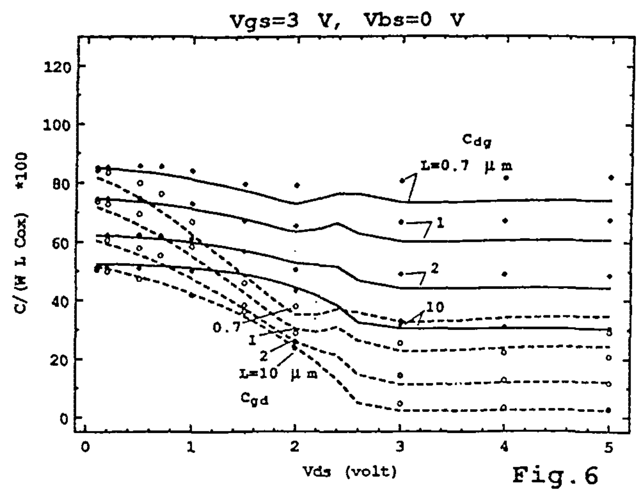

Fig.6

MEAN NORMALIZED ERROR %

channel length	Cgs	Cgd	Cdg	Cbs	Csd	Cdb	Cbd	Cbg	Cgb	MEAN
0.7	5.1	4.2	3.9	1.8	4.2	5.3	2.6	1.1	1.6	3.0
1.0	5.2	3.8	4.2	1.4	2.4	3.7	1.5	1.5	1.6	2.5
2.0	5.8	2.1	3.6	2.9	0.8	2.1	0.9	1.7	1.4	2.1
10.0	4.2	0.8	2.9	4.5	4.6	1.3	0.7	2.0	1.0	1.8