A Compact SPICE LDD MOS Transistor Model that Includes the Hot Electron Induced Substrate Current

*S. S. Chung, P.-C. Hsu and J.-S. Lee**
Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.
** The Winbond Electronic Corp., Hsinchu Industrial Park, Taiwan, R.O.C.*

Abstract - This paper describes a newly developed LDD MOS device model- *UNIMOS*, for circuit simulation in SPICE. It includes a consistent set of dc (I-V), and hot electron induced substrate current models. For the I-V model,new results for achieving accurate and computationally efficient models of both conventional and LDD MOS devices with submicron channel length will be described. In addition, development of the new hot electron induced substrate current model and the incorporation of the above model equations into SPICE useful as a measuring of the hot electron effect will be demonstrated with a practical example.

Introduction

Two basic models needed for circuit simulation in SPICE are the dc(I-V) and ac (C-V) models. These two MOSFET models in SPICE have been developed for years [1]. The Berkeley SPICE MOS models which have been evolved from LEVEL 1, 2 3 to a recent LEVEL 4-BSIM [2] version has shown wide applications for conventional MOS devices. However, there are limitations of the above models for submicron and even deep-submicron devices. It is also known that the substrate current ,I_B, can be used as a good monitor of the generated hot electron effect in a circuit during dynamic operations and has been ignored in SPICE simulation. Analysis of the device or circuit failure in particular the hot carrier effect which affects the long term reliability is becoming an important issue in VLSI design. We are in lack of a hot carrier model for SPICE so that circuit designer can use it to develop or optimize hot carrier resistant devices or circuits. Continuing efforts will be made to improve currently used dc models and the inclusion of the substrate current in circuit simulation using SPICE.

The present SPICE model includes a consistent set of I_D and I_B models. We suggest a revolutional equivalent circuit model of LDD MOS devices in Fig.1 which will meet the requirement of the drain current model for conventional circuit simulation and also the simulation of the generated substrate current during switching transient [3]. Usage of the modified SPICE simulator will be demonstrated with examples.

A Compact LDD MOS Device I-V Model

An improved model for the I-V characteristics of small geometry LDD MOSFETs was first developed based on the enhancements of our previous models in [4,5] and a newly-developed optimization algorithm. The expressions achieved for the drain currents hold in the weak inversion, strong inversion and saturation regimes of operation. Several major improvements in the newly developed LDD MOS device model include: (1) A gate voltage and drain voltage dependent properties of the drain-source series resistance, (2) Optimization of the model parameters which will enhance the accuracy of the model. This is more important for analog circuit applications. (3) Discontinuity problem of I-V curves at the near threshold region in the original SPICE model is also solved in the new model.

The drain-source series resistance effect in LDD devices is crucial. In the present approach, an LDD MOS device can be considered to be an intrinsic MOS device in series with two explicit resistors as shown in Fig. 1. These two drain-source resistances are the first to be derived as functions of gate- and drain-voltage, in which the gate voltage dependent feature is obtained as shown in Fig. 2. Suitably chosen boundary conditions are derived to get a better approximation of this resistance effect in the linear region and guarantee the continuity of I-V curves at the saturation point. Accuracy of the I-V curve is enhanced by an optimization of the two mobility degradation factors θ and η, which will determine the accuracy of I-V curves in the linear region. Fig. 3 shows the modeled result for a set of (θ,η) after optimization. Comparison between model and experiment is shown in Fig. 4, in which excellent agreements has been achieved. Smooth transition at near threshold (Fig. 5) is also obtained which can speed up the convergence in circuit simulation and hence saves CPU time. Only *12 model parameters* are used to fully adapt the small geometry I-V models to a given process. In addition, benchmark test of a ten-stage inverter shows that a saving of 30% in CPU time has been achieved which further indicates the efficiency of the new model. An RMS error less than 5% can be achieved for the I-V models as seen form the comparison in Fig.5.

A New Hot Electron Model of MOSFET's In SPICE

The substrate current, I_B, model is basically a combination of the Lucky-electron model and the previous drain current model parameterized from the measured data. The substrate current, I_B, model uses the form similar to that in [6] and with minor modifications along with the device I_D model equations was summarized in Table 1. In the model equation, α_i and β_i are the impact ionization coefficients and l_c is the effective impact ionization region length. By doing measurements on a set of different channel length devices and plotting $\ln[I_B(V_{DS}-V_{DSAT})/I_D]$ versus $1/(V_{DS}-V_{DSAT})$as shown in Fig. 6. α_i as function of channel length can be found as shown in the insert of Fig.6. Comparison between model and experiment of the fitted I_B results for various channel lengths are given in Fig. 7, in which excellent match has been achieved. The insert of Fig. 6 also shows the channel length dependence feature of the impact ionization rate, α_i, as well as the nonlocal effect which is not previously reported.

Once the models for I_B and I_D are established, these two model equations can then be incoporated into SPICE, from which devices' drain current and substrate current can be simulated at any instant of time can be evaluated. This substrate current will be generated during only switching as shown in one example followed.

Circuit Hot Electron Effect Simulation

One typical application for demonstrating the reliability simulation of a given sense amplifier circuit is illustrated as follows. Fig. 7(b) shows the simulated output waveform at the drain of M9, Fig. 7(c) gives the simulated I_B for every n-MOS transistors. It also provides us the information of the *substrate current generation* during switching transient such as that described by Hsu et.al. [3]. One very important implications from 7(c) is that transistor M9 is susceptible to the hot electron stress due to the observed larger I_B by comparing with the other transistors, and hence has shorter lifetime. However, the suppression of this I_B can be achieved by using a different transistor size (W/L= 4/1) whose I_B is also shown for comparison. This shows the efficacy of the developed simulator for optimum design of VLSI circuits.

In summary, for the first time, we add a new LDD MOS transistor model in SPICE that includes the hot-electron induced substrate current. The dc I-V model has been shown to meet the requirement of submicron VLSI's. We have also demonstrated a way of evaluating the substrate current generation using circuit simulation. The amount of generated hot carriers in VLSI circuits can be monitored and reduced through design optimization based on the present substrate current-based SPICE simulation.

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(1) Linear region $(V_{GS}-V_T>aV_{DSAT})$

$$I_D = \frac{\beta_0(V_{GS}-V_T-0.5aV_{DS})V_{DS}}{\{[1+\theta(V_{GS}-V_T)](1+\eta V_{DS})+R_t\{1-(V_{DS}-V_{DSAT})^2/V_{DSAT}^2\}\beta_0(V_{GS}-V_T-0.5aV_{DS})\}} \quad (1)$$

where

$R_t = RV_{dsat}/(V_{GS}-V_T-0.5aV_{DSAT})$ R: given in Fig.2.

$a = 1+ 0.5(K_1+K_3)g/\sqrt{\Phi_S-V_{BS}} -(K_2-K_4)$

$g = 1- 1/[1.744+0.8364(\Phi_S-V_{BS})]$

(2) Saturation region $(V_{GS}-V_T<aV_{DSAT})$

$$I_D = I_{d,sat}/(1-\delta L/L) \quad (2)$$

$V_{dsat} = (V_{GS}-V_T+aE_CL)/D - \sqrt{(V_{GS}-V_T+aE_CL)^2-2D(V_{GS}-V_T)E_CL/D}$

where $D = a(1-\beta_0 RE_CL)$ and $V_{DSAT} = V_{dsat} + 2RI_{dsat}$: terminal voltage

Table 1 Model equations of the drain- and substrate-current for n-MOSFETs

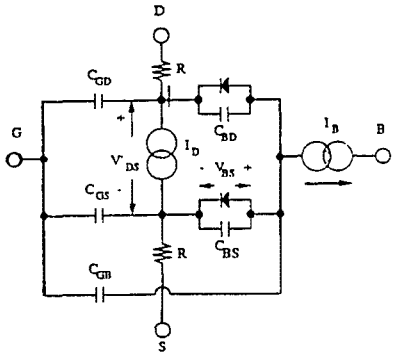

Fig.1 An equivalent circuit model of LDD MOS device in which a new substrate current model is added.

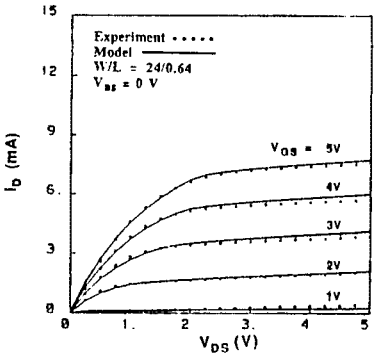

Fig.4 Comparison of the experiment and model for a short channel LDD MOS device.

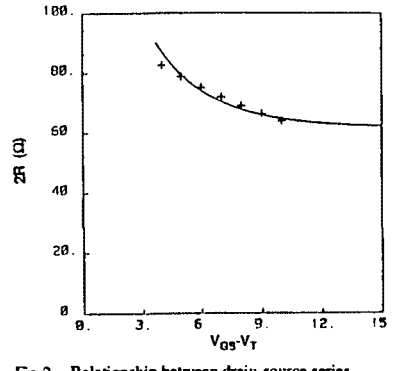

Fig.2 Relationship between drain-source series resistance and gate voltages. $2R = AL^{-n}+B$, A= 105, n= 0.36, B= 61.6.

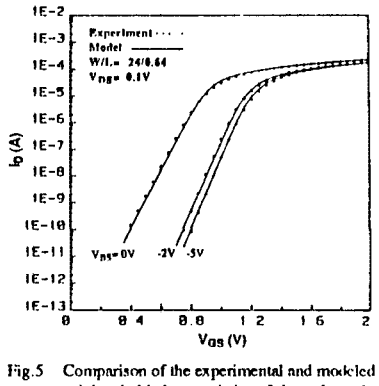

Fig.5 Comparison of the experimental and modeled subthreshold characteristics of short channel device.

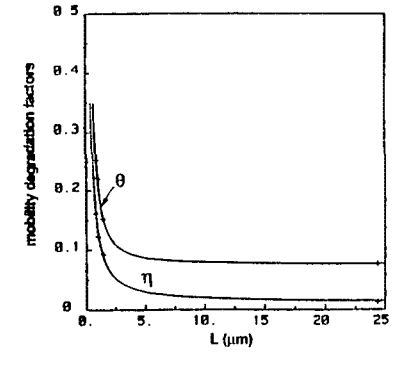

Fig.3 Optimum values of the mobility degradation factors versus channel length.

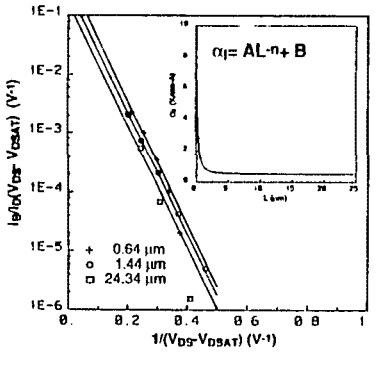

Fig 6 Characterization of the substrate current and the impact ionization rate α_i. The insert shows the channel length dependence of α_i.

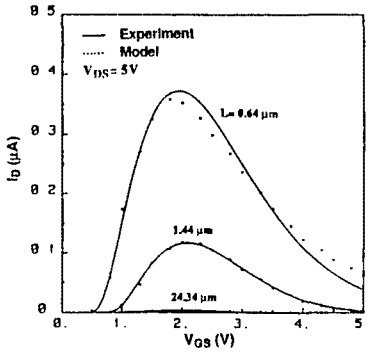

Fig.7 Comparison between the modeled and experimental data for the substrate currents of different channel lengths.

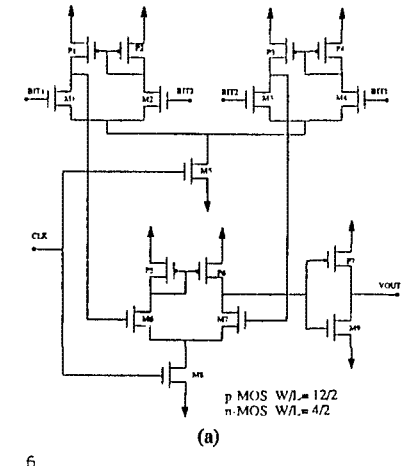

Fig. 8 A sense amplifier circuit for reliability analysis (a) The circuit, (b) Simulated output waveform, (c) Simulated I_B for each transistors.