Analysis of the Drain Breakdown Mechanism in Thin-Film SOI MOSFET's

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ABSTRACT

One important trend in recent years is the reduction of the silicon film thickness in SOI devices. As results of scaling this parameter several benefits have been obtained such as the elimination of the kink effect, the suppression of short-channel effects, improved subthreshold characteristics, the enhancement of carrier mobility, suppression of punchthrough and drain current overshoot and so on. These advantages mean that thin film SOI MOSFET's show great promise as high density and speed devices for future ULSI circuits.

However, as was already seen in recent experiments, it is a common fact that thinner film SOI devices exhibit lower drain breakdown voltages than thicker film SOI MOSFET's. Because thin film SOI devices seem to quite resistant to minority carrier accumulation and also suitable to the reduction of the peak electric field near the drain as had been seen in a lot of previous simulation works for understanding the kink elimination or the suppression of drain-current overshoot, it is difficult to explain the drain breakdown mechanism using the so-called parasitic bipolar action just like that in a bulk Si MOSFET directly. For a long time, there were no better models (especially analytical models)explaining the drain breakdown mechanism of thin film SOI devices. Lately, Yoshimi et al. suggested that the drain structure, rather than source structure, would play a major role in determining the drain breakdown voltage and that holes could accumulate near the source in the thin film devices at a higher drain bias. Although this is a reasonable explanation to the drain breakdown mechanism up to now, a more clear description of the physical process of the drain breakdown and a comprehensive analytical model will be needed for the analysis and design of SOI devices and circuits.

In this paper, the drain breakdown mechanism in thin film SOI devices has been analyzed in detail. The objectives of our work are to study the physical factor of determining the drain breakdown voltage and get a clear analytical model for understanding the drain breakdown phenomena. With the proposed analytical model, which takes into account the dependence of the drain breakdown voltage on biases and geometries such as film thickness and channel length of a SOI device, we can explain the breakdown phenomena of SOI MOSFET's and understand the relation between the kink effect and drain breakdown very well.

With a quasi-two-dimensional method, we have investigated the distribution of the lateral electric field near the drain region. It can be seen that the lateral electric field strength and the impact ionization factor M, which are the dominant factors influencing the impact ionization process, increase significantly with the decrease of SOI film thickness. Because the generation rate of minority carriers increases, rather than decreases, with the reduction of the film thickness of a SOI device, we suggested that a lot of minority

carriers ,which were generated by impact ionization near the drain, will be injected to source region under stronger electric field. And we call this process as drain generation process. In addition, we suggested that the minority carriers near the source can diffuse into the source region more easily because that the potential barrier height at the source/SOI-body junction is reduced as the SOI film thickness decreases.And we call this process as source diffusion process. Based on our analysis and simulation results , we considered that the drain current kink and drain breakdown voltage lowering are the results of a delicate balance between source and drain. If no source diffusion process occurs more holes will be accumulated near the source. This will result in same kink and breakdown characteristics as those in partly depleted devices.If the source diffusion process dominates over the drain generation process there are no holes accumulated near the source so that neither kink nor breakdown characteristics are observed.If the drain generation process dominates over the source diffusion process, a lot of holes will be accumulated near the source. At this time, a parasitic bipolar action similar with that in a bulk Si MOSFET occurs and the device get breakdown.

Based on above discussion, we have developed a analytical drain breakdown model and studied the breakdown characteristics of thin film SOI devices in different conditions. The simulation results can explain the experimental phenomena observed so far. The simulated current-voltage characteristics for SOI devices with different film thickness show the significant lowering of the breakdown voltage in the thinner device. We have obtained the dependence of the maximum lateral electric filed strength Esd and the avalanche multiplication factor M at the drain on the SOI film thickness. It can be seen that Esd and M increase obviously with the decrease in SOI thickness. Also, we have studied the breakdown characteristics of an asymmetric device structure by supposing that the SOI film thickness at the source will only influence the initial potential barrier height at the source/SOI-body junction. The results indicate that the drain breakdown voltage is quite insensitive to SOI film thickness at the source. But, our results show that the occurrence of the kink effect is dependent on the film thickness at the source region.

With a detailed discussion on the relation between the kink effect and drain breakdown, we can conclude that occurrence of the kink effect is dependent on the initial potential barrier height at the source/SOI-body junction determined by the film thickness at the source region of a SOI device, and that the occurrence of drain breakdown is dependent on the lateral electric field strength at the drain determined by the film thickness at the drain region of a SOI device. Therefore, we could improved the drain breakdown characteristics of thin film SOI devices in the application of ULSI circuits by means of the optimization of SOI thickness and a proper choice of the power supply voltage or designing some new device structures.