A METHOD FOR THE ANALYSIS OF EPROM CELLS SCALING DOWN

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The scaling down of microelectronic components involves several criteria for the optimization of the device structure. Performance and reliability have to be simultaneously implemented, and even the operating voltage can be adapted to the requirements of a correct scaling.
The scaling strategy of EPROM cells down to the sub-half-micron range is determined by the analysis of a number of parameters, which characterize the performance and reliability of the individual component; cell writing speed, threshold voltage shift, cell break-down (including specific effects, such as drain turn-on, punch-through and band-to-band tunneling) and the maximum voltage supported by the process architecture concurr to the definition of the working area of a cell.
In this paper we propose a method, based on the simulation of the cell characteristics, to define the working area of an EPROM cell, and to analyze its operation in view of the fundamental criteria stated above.
The simulation of the writing characteristics for several bias configurations is performed by means of the 2-D device simulator HFIELDS [1], through the use of a post-processor that allows the calculation of hot carrier injection in the cell floating gate [2]. The writing speed and the threshold voltage shift are extracted from the writing curves, and the voltage settings which are consistent with the minimum operation requirements are determined.
These simulations are riported in fig.1 and fig.3 for a 0.4 um gate length cell. The simulation of the cell with grounded gate and high drain voltage conditions allows the identification of the maximum supported drain voltage, whereas the knowledge of the general process architecture determines the maximum supported gate voltage.
Given that the above cited parameters are known, one can sketch the working area of the studied cell in the Vd/Vg space as in fig.5, where each boundary is identified by the related criterion.
To verify that realistic results are produced by the proposed methodology, the working area of a 0.6 um gate length cell has been experimentally determined using the same method, by direct measurement of the electrical characteristics. The results are shown in figures 2,4,6; it can be observed that the experimental working area in fig.6 is qualitatively similar to the simulated one (fig.5); the comparison shows also that the scaling down of the dimensions allows the operation at reduced voltages. The analysis of the working area modification depending on the process related parameters, such as gate length, insulators thickness, doping profiles, etc. allows the optimization of the device structure and the study of the process latitude.

[1] - G. Baccarani, R. Guerrieri, P. Ciampolini and M. Rudan - Proc. of NASECODE IV, J.J. Miller ed., Dublin, Boole Press, pp.3-12, 1985

[2] - C. Fiegna et al. - Proc. of ESSDERC '90 - Nottingham (UK) 1990, p.527

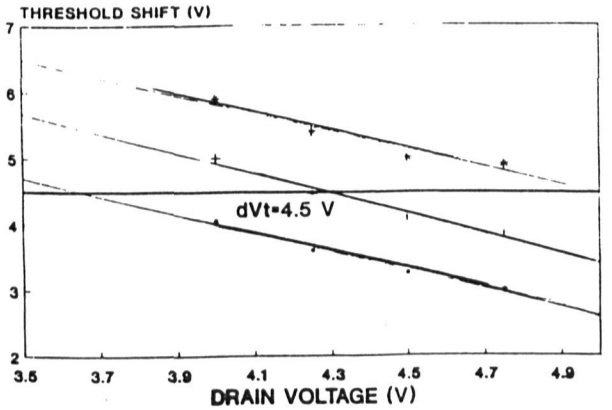

Fig.1: Simulated threshold voltage shift for Vg = 8.5 V, 9.0 V, 9.5 V. Gate length = 0.4 um. The minimum acceptation criterion is dVt > 4.5 V.

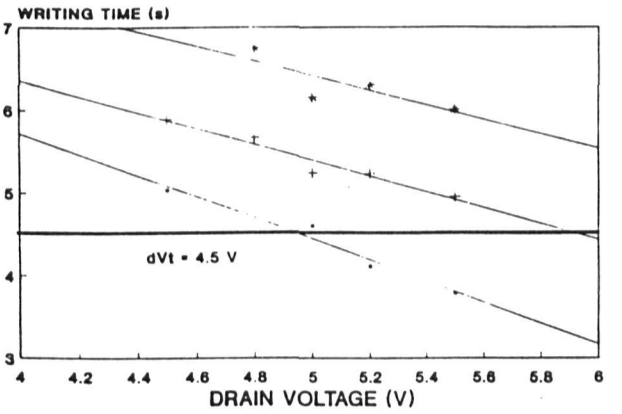

Fig. 2: Experimental threshold voltage shift for Vg = 10.5 V, 11.5 V, 12.5 V. Gate length = 0.6 um. Same criterion as in fig.1.

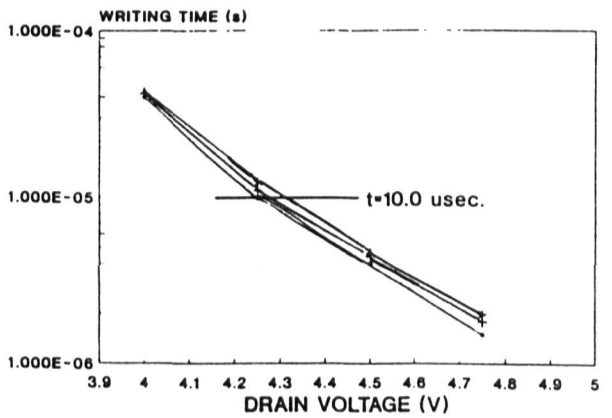

Fig.3: Simulated writing time for the same Vg conditions and device structure as in fig.1. The minimum acceptation criterion is t_w < 10 usec.

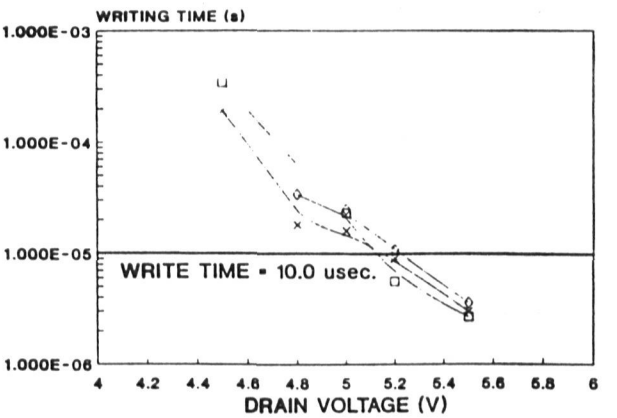

Fig.4: Experimental writing time for the same conditions, device structure and acceptation criterion as in fig.3.

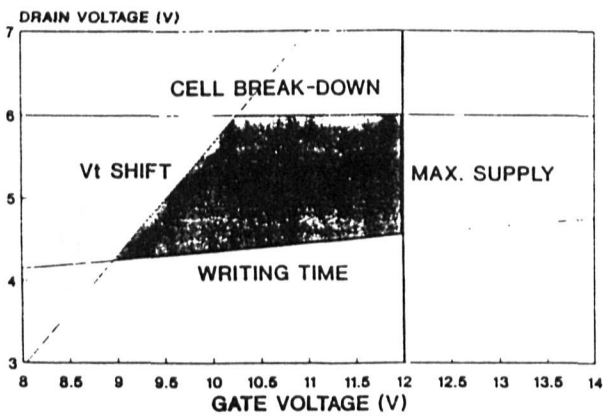

Fig.5: Working area of the simulated cell in the Vd/Vg space. The four boundary lines are defined by the criteria defined in the text.

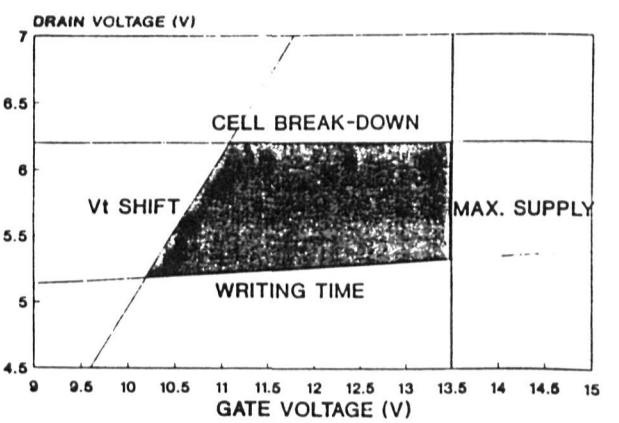

Fig. 6: Experimentally measured working area of the 0.6 um cell. The boundary lines are defined in the same way as in the simulated procedure.