A General Purpose Device Simulator Including Carrier Energy Balance Based on PISCES-2B

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1 Introduction

Continuing evolution of fine-pitch semiconductor devices into the deep-submicrometer region, with typical device dimensions of $0.5\mu m$ and smaller, forces a revision of the classically used numerical models. In very small devices the mobile carriers can no longer be assumed in thermal equilibrium with the lattice. In regions of high electric field carrier energy can be orders of magnitude higher than the one assumed by the classical drift-diffusion equations [1]. Physically accurate treatment of local carrier heating (and cooling) effects is generally expected to improve the predictive capabilities of simulation of small devices for which hot-carrier effects are increasingly important.

The following is a discussion of the self-consistent solution of the Poisson's, current continuity and carrier energy balance equations based on the general purpose device simulator TMA PISCES-2B[1]. The new model has been successfully tested for various devices including ballistic diodes, BJTs, bulk MOSFETs and SOI-MOSFETs.

2 The Hydrodynamic Model

The implemented hydrodynamic model includes the classical drift-diffusion set of equations for the electric potential and carrier concentrations [2]:

$$\nabla\epsilon\nabla\psi = -q(p - n + N_D^+ - N_A^-) - \rho_F \qquad (1)$$

$$0 = \nabla\cdot\vec{J}_n - qU_n, \quad 0 = \nabla\cdot\vec{J}_p + qU_p \qquad (2)$$

The generalized expression for the electron current density takes the thermal diffusion current into account, resulting from spatially inhomogeneous carrier temperature:

$$\vec{J}_n = -q\mu_n[u_T\nabla n + n(\vec{E} + \nabla u_T)] \qquad (3)$$

The carrier thermal voltage $u_T = kT/q$ is determined by the energy balance equation [3, 4]:

$$\nabla\cdot\vec{S}_n = \frac{1}{q}\vec{J}_n\cdot\vec{E} - \frac{3}{2}n\frac{u_T - u_T^0}{\tau_w} \qquad (4)$$

$$\vec{S}_n = -\frac{5}{2}u_T\left[\frac{\vec{J}_n}{q} + c_q\mu_n n\nabla u_T\right] \qquad (5)$$

The energy relaxation time τ_w has been chosen to be $0.4ps$. A carrier temperature-dependent mobility model [4] has been implemented, enabling a description of the velocity overshoot effect:

$$\mu_n = \frac{\mu_0}{1 + \alpha(u_T - u_T^0)}, \quad \alpha = \frac{3\mu_0}{2v_s^2\tau_w} \qquad (6)$$

3 Solution Strategy

A decoupled approach has been chosen for the self-consistent solution of the hydrodynamic model. That is a solution of the drift-diffusion eqs. (1-3) for the classical variables u, n, p, followed by a solution of the energy balance equation (4) for the electron thermal voltage u_T. The new temperature distribution is used to re-evaluate u, n, p. This procedure is repeated until updates of the temperature fall below a specified limit.

The convergence of the iteration is generally sufficiently fast. However, problems are observed at low current densities and for irregular or coarse grids. These problems appear to be related to insufficient accuracy of the current density. The behavior is similar to that of impact ionization models.

The discretization of the energy balance equation follows the box integration strategy on a triangular grid used for the drift-diffusion equations in PISCES [2]. Special care must be taken in the evaluation of the carrier heating term $\vec{J}_n\cdot\vec{E}$ in eq. (4). In the current implementation averaging over the entire triangular element is used rather than a scalar product along the sides.

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[1]TMA PISCES-2B^{TM} is a trademark of Technology Modeling Associates, California, USA

4 Application

An SOI-MOSFET with an effective channel length of $0.35\mu m$ serves as a test device to demonstrate the new hydrodynamic model. Fig. 1 presents the structure of the device and contour lines of the electron temperature calculated for bias conditions $V_S = 0V, V_G = 0.25V, V_D = 1V, V_{Sub} = 0V$. Maximum carrier heating to about $1910K$ occurs under the gate at the channel-drain junction.

Local carrier heating results in an additional thermal current in the hot area, significantly increasing the electron concentration in comparison to classical drift-diffusion models as shown in Figs. 2, 3. The new model predicts a substantially smoother electron distribution in the channel with higher carrier concentration in the high-field (pinch-off) part of the channel.

Availability of the carrier temperature is expected to greatly improve the description of important physical models for future deep-submicrometer devices. Further work will focus on model development and characterization for carrier mobility including velocity saturation and velocity overshoot effects, impact ionization, hot-carrier injection in the oxide, etc.

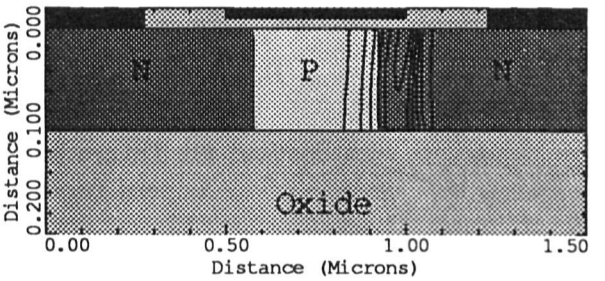

Figure 1: SOI transistor structure and electron temperature contour lines for $T = 250, 500, 750, \ldots K$.

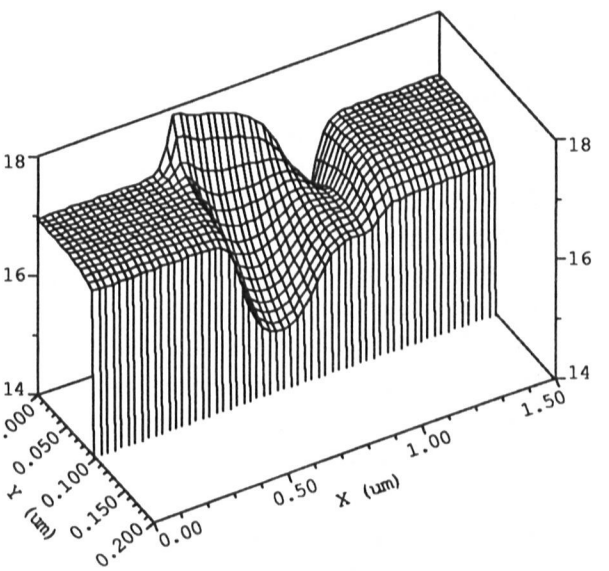

Figure 2: Electron concentration.

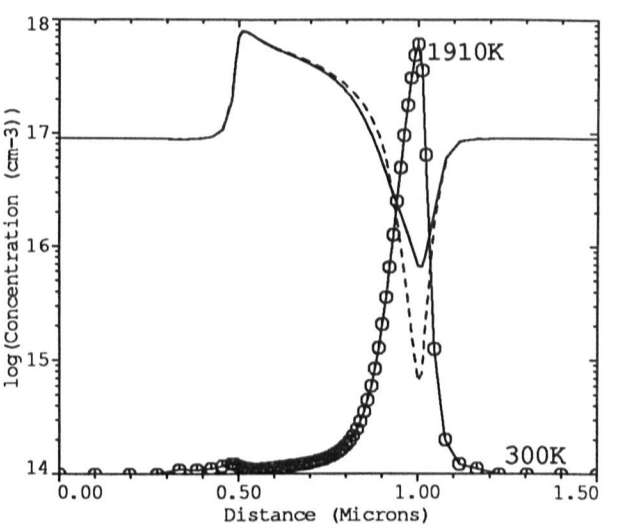

Figure 3: Electron concentration for the hydrodynamic model (solid line) and the drift-diffusion model (dashed line) as well as electron temperature distribution (circles) along the upper $Si - SiO_2$ interface.

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References

[1] W.V. v. Roosbroeck. Theory of flow of electrons and holes in germanium and other semiconductors. *Bell Syst. Techn. J.*, 29:560–607, 1950.

[2] C.H. Price. *Two-Dimensional Numerical Simulation of Semiconductor Devices.* PhD thesis, Stanford University, Stanford, California, May 1982.

[3] A. Forghieri, R. Guerreri, P. Ciampolini, A. Gnudi, M. Rudan, and G. Baccarani. A new discretization strategy of the semiconductor equations comprising momentum and energy balance. *IEEE Trans. on CAD*, 7(2), Feb. 1988.

[4] B. Meinerzhagen and W.L. Engl. The influence of the thermal equilibrium approximation on the accuracy of classical two-dimensional numerical modeling of silicon submicrometer mos transistors. *IEEE Trans. on Electron Devices*, 35(5):689–697, May 1988.