Development of a unified process and device simulation environment —P&D Workbench—

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1. Introduction

In order to reduce VLSI device development time, process and device simulators are now widely used. However, it imposes a heavy burden upon a designer to manage data and jobs of various simulators. In order to improve this situation, several integrated simulation systems have been developed so far [1-5]. However, user interfaces are not specifically described in some papers, [1,2], and the computer environments for the numerical simulation are not described in detail in other papers [4,5]. An integrated simulation system can have an excellent user interface if an EWS (Engineering Work Station) is adopted as a front-end processor. On the other hand, it is not always efficient to execute process and device simulations on an EWS, and a high performance back-end processor should be used [3]. However, if a MFC (Main Frame Computer), which is not always so associative with an EWS, is adopted as a back-end processor, there still remains a problem in efficiency and usability. In this work, we developed a supervising simulation system (*Process & Device Workbench*), that integrates process and device simulators in order to provide both an excellent user interface and a smart numerical calculation environment.

2. System Outline

In P&D Workbench, front-end processes are executed on an EWS and numerical calculations are executed on either an EWS or a MFC that can be selected by a user in consideration of a problem size. P&D Workbench has X-window based excellent user interfaces, and consists of a data input module, an automatic job execution system, a data/job management system and a result display system with color graphics. Figure 1 shows a block diagram of the system. P&D Workbench is implemented on "Master EWS" and is connected with other EWSs and MFCs via networks and a gateway computer which can convert different network protocols. This gateway acts as a virtual TSS terminal for a MFC, and it spawns a remote job to a MFC according to the request from P&D Workbench. P&D Workbench can inquire the job completion and the execution report is transferred from a MFC to an EWS through the gateway. Our supervising system manages all the data files and the executed jobs on both an EWS and a MFC. Therefore, a user does not need to input any computer command after entering P&D Workbench. All the operations can be done only by clicking a user-friendly menu filled with Japanese process terminologies. Available simulators on P&D Workbench at present are two-dimensional process/device simulators, a topography simulator and a capacitance simulator.

DAIJOBDA is a data input module, which prepares an entire simulation recipe from a process sequence data to a device analysis data. SPARTAN is a 2D-process simulator, which has implantation, oxidation, diffusion and stress simulation capabilities. BIUNAP is a general purpose 2D-device simulator, which can handle arbitrary device structures, and has an interface program which converts a SPARTAN's mesh configuration to a one suitable for device simulation. VMAP is a topography simulator, which simulates 2D-topography according to a process and a mask layout data. STORK is a 2D-capacitance simulator, which calculates wiring capacitances of a structure produced by VMAP. VDP-CORE visualizes all simulation results on a color graphic window.

3. Application and Performance

Figure 2 shows a simulation result of n-ch LDD-MOSFET by P&D Workbench. Section(A) is the main menu of the supervisor in P&D Workbench. It manages an input step of a simulation recipe, an executing step, a visualization step and EWS/MFC jobs, and also displays the CPU load of a MFC. First of all, a user makes a simulation recipe which consists of process conditions and device analysis data. Since P&D Workbench has several standard recipes in a data-base, it is enough for a user only to modify them whenever it is necessary. Section(B) shows an example of a process sequence data on DAIJOBDA. Section(C) shows a device current table simulated by BIUNAP and section(D) shows a potential distribution visualized by VDP-CORE. Figure 3 shows an example of a topography simulation followed by a capacitance simulation. Section(E) shows a topography simulation result by VMAP. In VMAP, a user specifies an arbitrary cutline in a mask layout and then the device topography is simulated along the line with process data given by DAIJOBDA. Furthermore, the topological data is transferred to STORK and wiring capacitances are calculated. Section(F) shows a capacitance table simulated by STORK and section(G) shows a potential distribution visualized by VDP-CORE. Figure 4 shows the throughput of the entire process and device simulations when P&D Workbench is used. When a MFC is used, the overhead time, which is a sum of data transfer time, file existence check time, waiting time for execution and results transfer time, occupies 30min in the entire simulation time (36min). On an EWS, the execution time costs 72min, and the overhead time is negligible. It can be expected that for a smaller problem

the throughput of an EWS tends to be faster than of a MFC because of the negligible overhead time.

4. Summary

P&D Workbench has an excellent user interface and provides a smart numerical environment. VLSI device designers can use process/device simulators very efficiently by means of this system. In the future, EWSs will be connected with MFCs directly, not via a gateway computer, in order to reduce the overhead time, and three-dimensional process/device simulators will be added by taking advantage of the flexible expansibility of this system.

References

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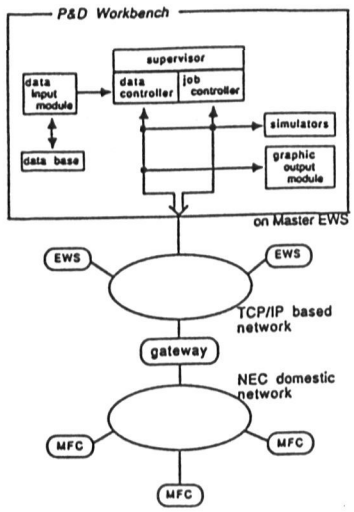

Figure 1. Block diagram of P&D Workbench. EWSs are connected with TCP/IP based network and MFCs are connected with NEC domestic network. Furthermore, two different networks are connected via a gateway computer. Process/device simulations are executed on either an EWS or a MFC.

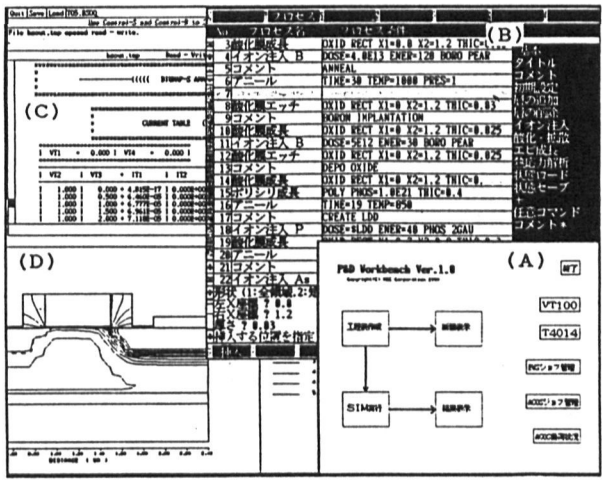

Figure 2. Simulation result of n-ch LDD-MOSFET by using P&D Workbench. Section(A) is the main menu of P&D Workbench, section(B) is an example of process sequence data by means of a data input module, section(C) shows a device current table and section(D) shows a potential distribution.

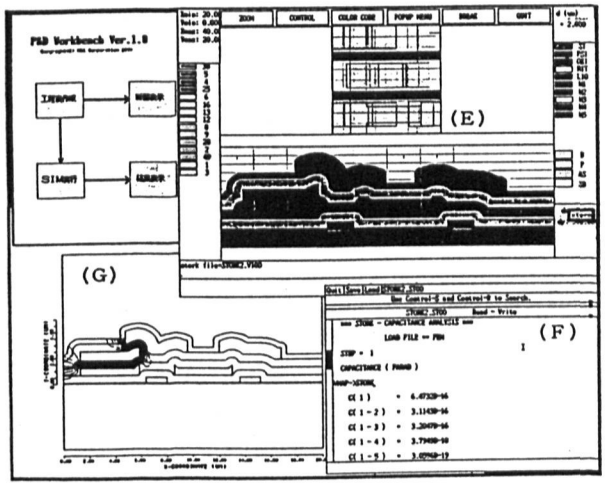

Figure 3. Simulation result of a device topography followed by a capacitance simulation. Section(E) shows a topography simulation result, section(F) shows a capacitance table, and section(G) shows a potential distribution.

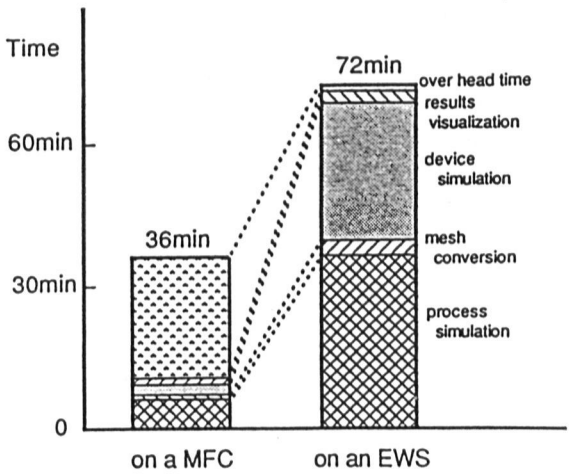

Figure 4. The throughput of the entire process/device simulations by means of P&D Workbench.