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# Modeling of Alignment Schemes In Commercial Steppers

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## Summary

As modern integrated circuit design has marched well into the submicron regime, tighter controls need to be placed in photolithography processing. Very often the most difficult task in photolithography is not in manufacturing submicron photoresist features, but in accurately aligning the reticle to the wafer in order to cope with the stringent design rules. This is especially true as the topography on the wafer surface becomes more complex so that the alignment mark on wafer (i.e., wafer mark) can be degraded easily by various etching and deposition steps. The visibility of the wafer mark is further obscured by the coated resist layer which may be nonplanar and asymmetric, thereby causing an alignment offset. Another factor that prohibits engineers from manufacturing the optimum wafer mark is that vendors have devised and implemented different alignment schemes into their steppers so that the alignment has become a totally equipment-dependent problem. Wafer mark with unique structure and dimensions has to be designed for each specific scheme on a stepper. With these puzzling factors, there is a need to model these commercial alignment schemes in order to help process engineers and optics designers understand this bottle-neck problem better.

The scattering model employed to solve the light scattering problem in wafer structures is the "wave-guide" model[1,2,3], which rigorously solves the Maxwell's equations. The imaging model employed to model different alignment imaging systems of steppers is based upon the Abbe's imaging theory. A simulator based on these models has been implemented. It can be used to study how different alignment systems perform under wafer marks of arbitrary topography, and to further develop optimum alignment marks.

Two examples to demonstrate the applicability of our simulator are given below. For the LSA scheme used by Nikon steppers, grating-type alignment marks are manufactured on the wafer and scanned across a stationary laser spot as shown in Fig.1(a). The diffracted light is collected as the alignment signal and maximum signal intensity is detected when marks are fully exposed under the light spot. The peak intensity, however, strongly depends on the ratio of the line and space and the specific profile of the coated photoresist layer. Experiments were carried out[4] by utilizing $3\mu m/5\mu m$, $4\mu m/4\mu m$ and $5\mu m/3\mu m$ ratioes and it was discovered that 4/4 yields the maximum intensity. Simulations of the same experiments were performed and the verification result is shown in Fig.1(b). Furthermore, it was found that the optimum ratio for the specific topography of interest is 4.25/3.75. For the key target convolution scheme used by Ultratech steppers shown in Fig.2(a), experiments were carried out[5] to study the alignment problem when aligning at the aluminum level. It was discovered that when the oxide mark height exceeds, say $1\mu m$, the single-peak well-defined alignment signal becomes multi-peak and vague. Simulations were also performed in this case and the same trend can be repeated as shown in Fig.2(b).

One major source of alignment offset due to topography is the asymmetric resist coating on the wafer mark. Here, simulations were been performed to study this effect for different commercial alignment

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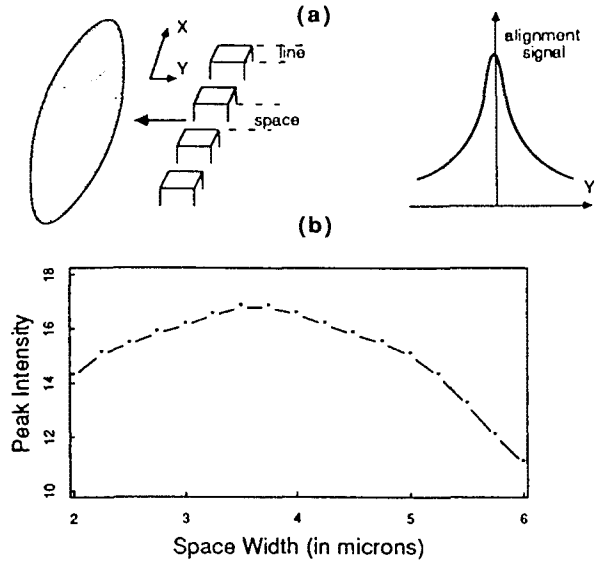


Figure 1: (a) Nikon alignment scheme. (b) Peak signal intensity vs. width of the grating space.

schemes that can be modeled using our simulator, as shown in Fig.3. The bright field scheme is employed by some of the Censor and Hitachi steppers. When the coated resist profile is planar, the alignment signal is symmetric and it is easy to determine the center (or the alignment position) of the signal. However, this scheme is very sensitive to thickness variations so that the nonplanar resist coated on top of the mark can drastically alter the shape of the signal and cause an alignment offset. The GCA dark field scanning scheme employs two transparent reticle windows corresponding to the edges of the wafer mark. The maximum signal occurs when perfect alignment is achieved. The Canon dark field scanning scheme generates signals corresponding to the edges of the wafer mark, thus detecting the position of the wafer. The ASM Moire interference scanning scheme utilizes gratings as the reticle and wafer marks. Moire interference pattern is generated when overlapping these two grating images so that their relative position can be distinguished. Note that none of the schemes mentioned above can be exempted from alignment offset caused by asymmetric resist coating. By having the capability of modeling these schemes, engineers can distinguish the effects of topography variation on alignment offset and to modify their processes to improve alignment accuracy.

## References

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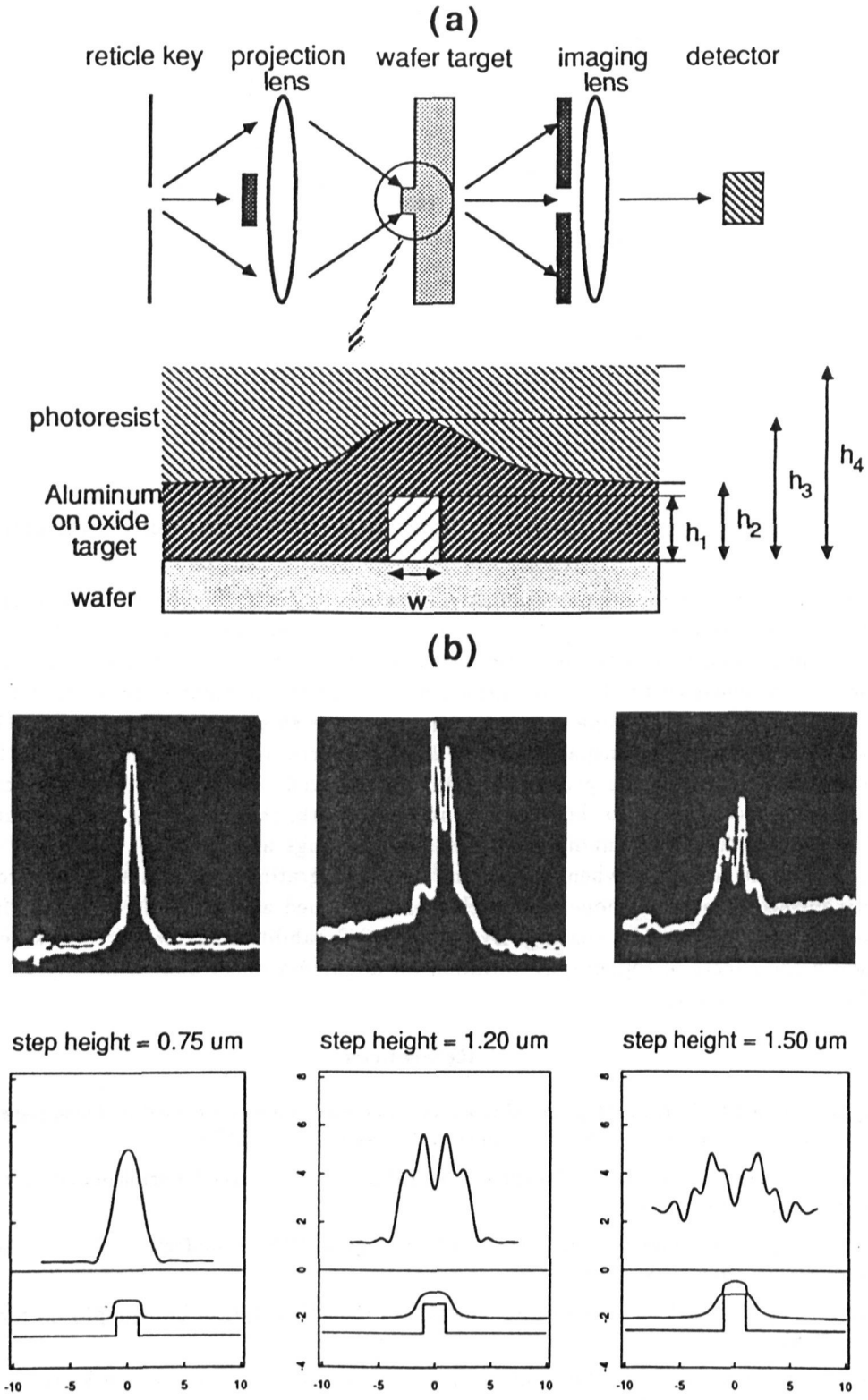


**Figure 2:** (a) Ultratech alignment scheme. (b) Experimental vs. simulation results for alignment mark of different heights.

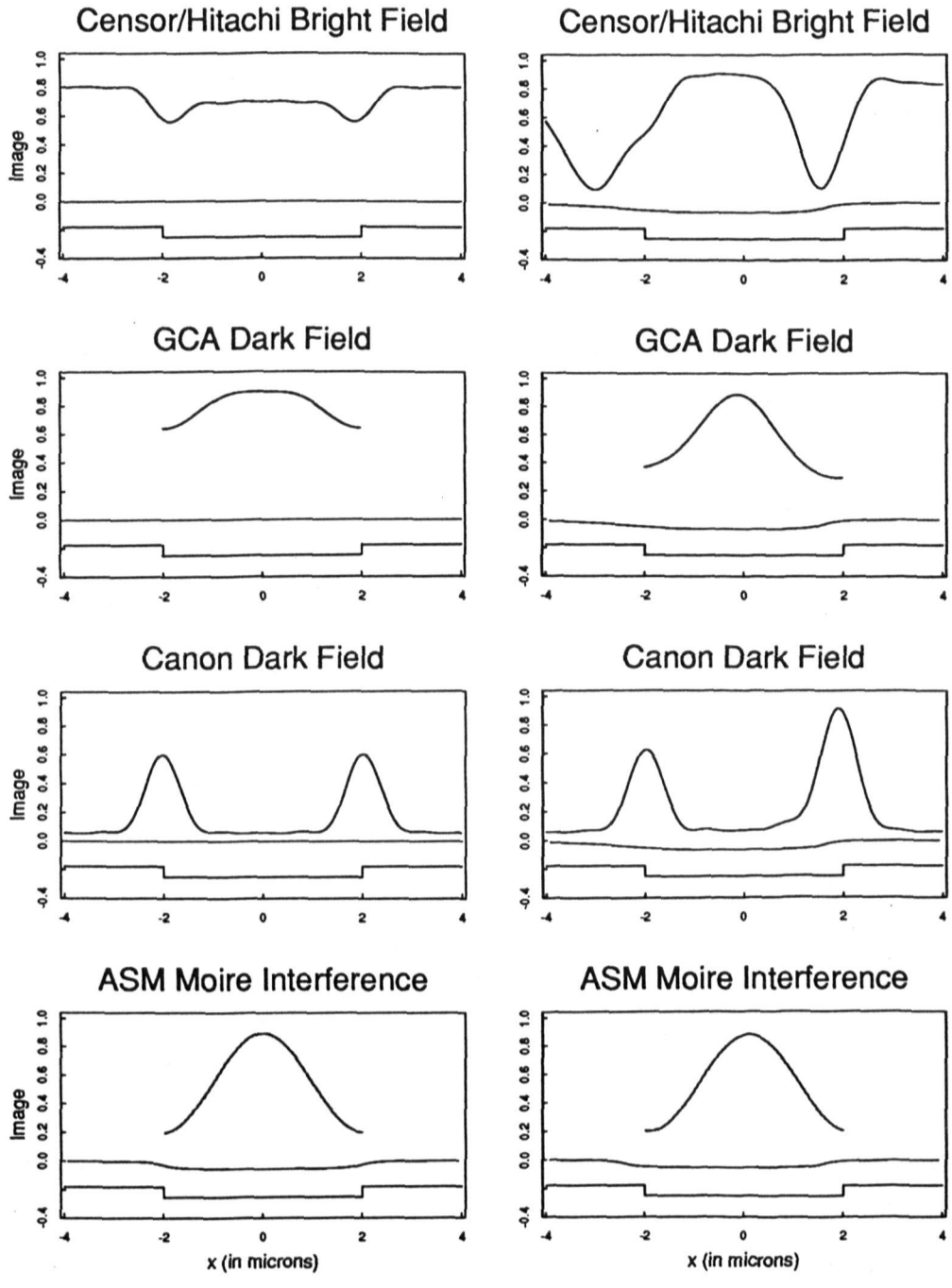


Figure 3: Simulated alignment images from schemes used by Censor, Hitachi, GCA, Canon and ASM steppers.