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Recent progress in understanding hot-carrier degradation: new assignments for modeling investigations?

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ABSTRACT

This paper describes the present status of understanding hot-carrier effects. This understanding is applied in the real operating environment, where the stability of a technology in general or of a specific product must be assured. From this, conclusions concerning lifetime criteria and related characterization methods are drawn and new modeling assignments outlined.

I. Introduction

After the relevance of the hot-carrier problem for MOS products had been discovered in the late seventies, a major world-wide effort was initiated to understand the phenomena relating to the destructive properties of hot-carrier effects. In the meantime we have achieved a rough, if largely only qualitative understanding of the phenomena encountered in n- and p-MOSFETs. This understanding will now be described. We also demonstrate its applications in the circuit environment and show that it is needed for a proper treatment of the obvious reliability problems. We emphasize that important open questions still remain, firstly concerning a quantitative description and secondly in explaining the apparent dynamic stress-related phenomena. For these, we hope to obtain considerable aid from the simulation side.

II. The physical understanding

The picture described below has been developed mainly on the basis of inhomogeneous stresses of MOSFETs monitored by electrical current characterization [1,2], charge pumping investigations [3] and device simulation [4]. However, gated diode currents [5] and homogeneous stress [6] have also contributed important detailed information.
In both channel-types, the degradation is dominated by drain-side effects as the highest lateral electric fields occur there, in the vicinity of the channel to the drain pn-junction (extending about 0.1µm [5]). These are largely a function of the drain voltage and the degradation consequently increases by more than an order of magnitude per volt increase in drain voltage. For constant drain voltage, the degradation peaks at low to medium gate voltages where the drain current has achieved a considerably high value (going from low to high V_G) and the lateral electric field is still high [7]. In the afore-mentioned maximum stress condition, the vertical field at the highest field location in the silicon and the oxide field both favorize hole injection in the n-channel and electron injection in the p-channel MOSFET. The situation can be altered at high gate voltages as the vertical electric field attains a lower value or even goes to the reverse direction. Furthermore, there is an important asymmetry in the barriers of oxide injection of electrons and holes, the second being much higher than the first. These considerations lead to holes and electrons being injected in the n-channel MOSFET, the number of injected holes decreasing much faster with increasing gate voltage than that of electrons.
As far as the electrons are concerned two different degradation modes can be distinguished by an examination of the time dependence of the degradation. (Fig. 1). For medium gate voltages injected electrons are thought to trigger the generation of interface states [3], while the change of the slope at high gate voltages was ascribed to electron-trapping [13]. The latter effect is strongly dependent on the processing line and often much weaker than shown in Fig. 1.
Degradation by hole injection is observable following stress at low gate voltages. It can be evidenced by a change in the slope of the lifetime vs. substrate current plot [3], when a definition based on charge-pumping is used, and by a shoulder in the charge-pumping current (Fig. 2) (for a description of the method see [8]). The shoulder is caused by the trapping of holes forming fixed positive charge. It causes the local threshold voltage to decrease, leading to a drain current increase and an electric field decrease. Another feature can be observed in Fig. 2: the density of interface states increases by a considerable amount [3]. These are of acceptor-type, leading to negative charge if energetically below the electron Fermi level; however, their effect is concealed by that of the positive charge and they were thus not recognized for a long time. They immediately become evident as soon as the holes are neutralized, which can be accomplished by a short hot-electron injection at high V_G. This process of positive charge neutralization by electron capture is very efficient. It leads to a further, but small increase of the interface state density. But most of the interface states are still formed during the low-V_G stress, at the hot-hole injection condition.

The process of interface state generation by holes is several thousand times more efficient than by electrons forming interface states directly without the help of holes [3,6]. However, as the number of injected holes decreases much faster than that of electrons for increasing V_G, above V_G=3-6 V the interface state generation by electrons dominates and can, in some technologies, also lead to the creation of fixed negative charges. The subsequent injection of holes and electrons described above is not of purely academic interest; it plays an important role in real circuit operation, as discussed below.

For decreasing drain voltages the electric field decreases and we expect the hole effects to disappear completely. However, measurements down to V_D=6V show the above-mentioned effect of interface state concealment in conventional n-MOSFETs which we count as an indication of hole trapping. The situation is, however, relaxed in modern LDD (low doped drain) devices where lower electric fields occur. Furthermore, a series resistance effect arises due to the electric field reduction by negatively charged interface states in the spacer oxide, which are not controlled by the gate. The time dependences are changed somewhat, leading to a tendency to saturation, but the mechanism described above holds.

On the basis of hot-electron injection alone C. Hu [9] developed a simple formula which is of great help for practical purposes and will be used later. It was shown [7] that its dependence on the specific model is weak. It can thus be used at least in some important limiting cases if it is written in the form $\tau = C\, I_{sub}^{m}/I_D^{m-1}$, where τ is the lifetime, C is a technology constant and m is a fitting parameter with a value of about 3.

The situation encountered in p-MOSFET is much easier to understand. Due to an opposing electric field for most stressing conditions, holes have practically no chance of being injected into the oxide. Only electrons are injected and cause the formation of negative fixed charge and interface states, the latter being invisible again, for similar reasons to those described in the n-channel case. Under the influence of external electric fields, the negative charges show detrapping effects [14] which may lead to consequences in circuit applications.

III. Application for the case of real device operation

Ever since the beginning of investigations into device-related hot-carrier effects, the reliability of the product was the central concern and now that we have achieved a basic understanding we return to the demand for long-term operation under well-defined operating conditions. Before going into the details of this investigation, we have to check whether new physical phenomena coupled with the time dependence of the applied voltages need be considered. Firstly, the question of the inherent time constant of the device is raised. An estimation of the transition time, assuming typical values for the mobility μ, the voltage drop V_D, and the junction depth x_j, yields $x_j/\mu V_D$ ~ 20-30 ps. This value means that the device is able to follow an external voltage change within 20-30 ps. For voltage changes in this time regime, the switching-off of the gate voltage would lead to a certain number of carriers in the high-field zone whereas no such carriers are expected during stationary state. These carriers could then be heated in the field, be injected, and cause an additional degradation. The fastest applications, however, have a delay per stage of the order of a hundred picoseconds and are thus probably not affected significantly by this effect. This is even more so for most experiments performed to date on externally fed devices and stages where transients of down to 3 ns are achieved. We cannot, therefore expect to observe intrinsic transient effects in these experiments. This was confirmed by work in which transient device simulation and substrate current measurements on pulsed devices were compared [10].

While the inherent time constant of devices will not represent the major problem, interface state related phenomena, with time-constants of the order of nanoseconds to milliseconds appear possible. They should show up in a similar way as the above-described effect, however, for longer times. Results by Igura et al. [11] and Weber [12] have been interpreted in this sense. However, investigations during recent years of well-developed LDD devices with low interface-state-densities and fields reduced by weak drain doping profiles have not shown any obvious enhancement effects, whereby the error bars of these experiments had still factors of nearly one order of magnitude in their lifetimes [12].

Evidence shows that charge-detrapping effects of electrons and holes can also play a role. Furthermore, the hopping conduction of holes in gate oxides could present a problem. All these effects are still under investigation, with results being expected in the near future.

One dynamic enhancement effect, however, the one due to voltage combinations, will be discussed in more detail here, as its evidence clearly affects operation-related lifetimes. While under static stress, at least for short stress times, only one injection condition of holes and electrons occurs, a dynamic stressing condition contains a variety of injection conditions. Low (1V) and high (4-8V) gate voltages occur during high drain voltage conditions (see insert in Fig. 3) so that hole and electron injection conditions appear within one cycle. During hole injection, interface states and positive fixed charge are formed. If the stress is a static one the positive charges reduce the electric field close to drain. This leads to a weaker time dependence than for a

dynamic stressing condition in which the holes are neutralized by injected electrons at high gate voltages (Fig. 3). This picture was tested by substrate current measurements. As the electric field is related to the substrate current, we expect a lower substrate current after stress in the case of a static stress. This is in fact found (Fig. 4), whereby the substrate current decreases in both stressing cases due to LDD-related series resistance effects. The decrease is, however, more pronounced for the static case in agreement with the above interpretation.

The effect described shows that quasi-static calculations of dynamic lifetimes $\tau \sim < I_{sub}^{m}/I_{d}^{m\ 1} >$ [7, 11] (< > represents a time average) can become erroneous if uncorrected for possible transient effects and the effect of voltage combinations. For this reason, we describe below an empirical method by which the stability of a product can be assured under the usual dynamic operation conditions. By performing dynamic stress tests on various kinds of circuits such as NAND and NOR stages, as well as inverters with big and small loads, we found that the degradation differs only by a relatively small amount (Fig. 5), in agreement with the above dynamic degradation-based lifetime formula. An estimation of the ratio of dynamic versus static lifetime yields a factor of 100 for the afore-mentioned applications, whereby the usual design rules must be observed. This investigation does, however, not include specific applications like the transfer gate which is stressed both at source and drain, certain circuits specifically used in DRAMs with bootstraps, and analog applications. All these need special attention, not only with respect to their degradation behaviour but also with respect to their lifetime criteria which are relaxed considerably in many cases (static transfer gate) but are enforced in others (analog applications). The method of individual measurement of different kinds of circuits described above seems complicated due to the considerable number of possible applications. However, it is at present the only one allowing quantitative and conclusive statements to be made about the hot-carrier stability of a process.

III. Conclusion

In the first two sections, a picture of operation-related degradation mechanisms was developed. However, this picture largely lacks the quantitative verification. As the limits of simple analytical calculations are quickly reached, 2-D simulation, and in some cases circuit simulation within the framework of rate equations for a description of oxide degradation, is demanded. The problem is highly two-dimensional because holes and electrons are injected into the oxide very inhomogeneously and possibly at different locations of the interface. Consequently, different distributions of fixed charges and interface states can result as a function of position. The distribution of the damage will, moreover, change for both different gate voltages and drain voltages. Furthermore, in the dynamic cases the injection conditions change as a function of time as the stressing voltages change. Thus there is a demand for modeling oxide degradation with a strictly limited number of free parameters but taking into account all available experimental material. In Fig. 6 an example for the kind of work demanded is shown. Here, linear-mode and saturation-mode drain currents and substrate currents were characterized in forward and reverse directions before and after stress. All data were used together to calculate the damage induced by hot carriers [4]. With a large amount of experimental data and a small number of free parameters, a reliable result is achieved this way. We need a similar method to check on oxide degradation mechanisms, including the time dependences of static and dynamic stressing results.

The demand for a qualitative and quantitative understanding of the degradation mechanism is not justified merely by an interest in acquiring basic knowledge, but it can also help to find suitable lifetime criteria for a process development at a time when a product is not yet available although single devices and small circuits function properly. It is then important to take the right measures to assure the lifetime of later products. In this, the approach of optimizing the hot-carrier effects may not be optimal for the whole process, because other important aspects could suffer, causing punch-through and manufacturing cost problems (due to an overly complicated process). Our ultimate goal is to obtain a precise knowledge of the hot-carrier problem and to weigh it against independent problems like oxide breakdown or even particle problems, in order to achieve the highest possible yields.

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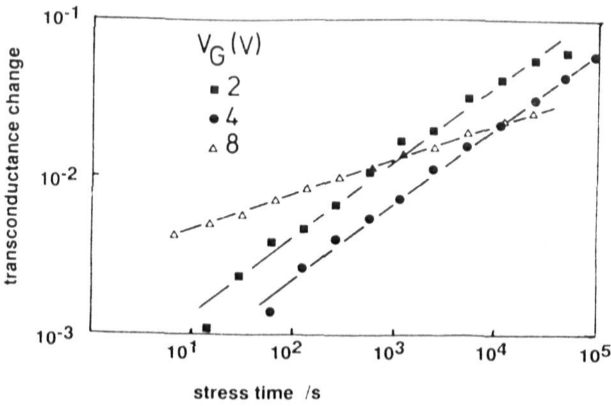

Fig. 1 Different time dependences of the transconductance after stress at low/medium and high gate voltages

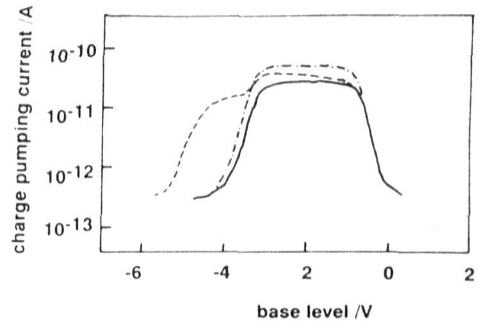

Fig. 2 The charge pumping current before stress (full line), after hot-hole stress (dashed line) and after subsequent hot-electron stress (dashed dotted line)

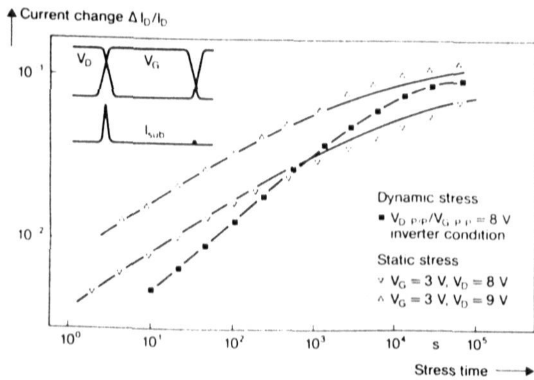

Fig. 3 The effect of varying voltage conditions in a dynamic stressing experiment compared with static conditions

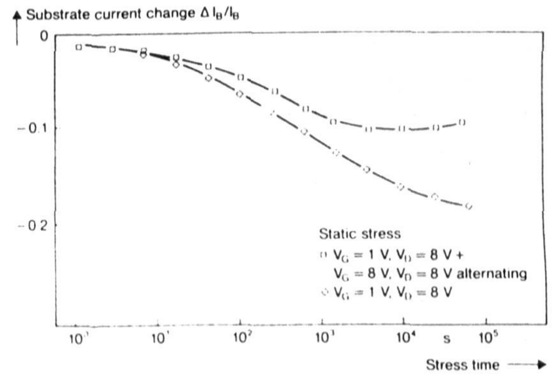

Fig. 4 Substrate current of an LDD n-MOSFET as a function of stress time for a static and an alternating stressing condition

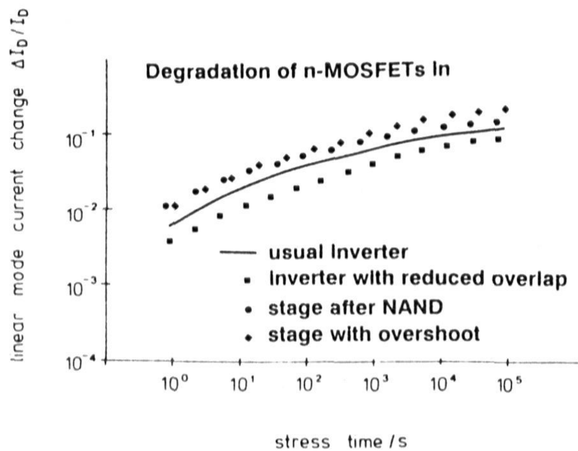

Fig. 5 Time dependences of hot-carrier degradation after different circuit-oriented stressing conditions

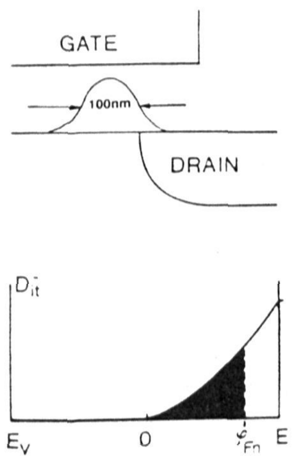

Fig. 6 Space- and energy-resolved distributions of hot-carrier induced interface states from a 2D simulation