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7min. talk

A Study of 3D Device Description and its Delaunay Partitioning

Masaaki TOMIZAWA, and Akira YOSHII
NTT LSI Laboratories
3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan
Phone: +81-462-40-2149, FAX: +81-462-40-4306

Abstract

The parasitic elements such as peripheral capacitance and resistance degrade the device performance with the reduction of the device size. For such a small-sized device design, it is necessary to take the three-dimensional (3d) device shape into account in device modeling. Therefore, an efficient algorithm for the 3d-device shape input and 3d-element partitioning are acutely needed. In this paper, we have investigated a user-friendly algorithm of such input and partitioning suitable for 3d-device modeling.

In the process of the constructing the 3d-device shape, it is imperative that the interactive input and modification can be easily and also frequently done by users. To facillitate a user-friendly construction, we use an engineering workstation. Furthermore, data structures, which describe 3d-device shape are hiearachically composed from vertices to regions. Therefore, in our approach, a user inputs only 2d-device cross-section data at each of the 3d-coordinates with a pointing device (mouse). The 3d-device shape is capable of automatically constructed with the interpolation of each 2d cross-section data at the specified 3d-coordinate. Figure 1 shows a typical input process for a 3d-device shape, and Fig.2 shows the data structure. With this approach, most semiconductor devices can be constructed in a user-friendly manner.

Furthermore, 3d-element partitioning suitable for the discretization of basic equations are investigated. First, grids are distributed tetragonally in the specified 3d-device, in which there are always grids on the vertices. Successively, a hypothetical body larger than the 3d-device is constructed using grids distributed in the device; then body can be partitioned by turns with tetrahedral elements based on a Delaunay partitioning[1], in which there are no grids within the circumsphere for each element. Finally, all of elements including the hypothetical grids which compose the body are deleted. Using this process, a 3d-device can be partitioned with tetrahedral elements. These elements provide great flexibility in the device geometry and are also suitable for the finite element method as a discretization of the 3-d differential equations. Figure 3 shows typical 3d-partitioned-elements using this partitioning algorithm. Table 1 is an example using these elements, in which we have successfully discretized Poisson's equation and calculated the 3d-wired capacitance by the finite element method as shown in Table 1.

References

[1] M.Sever: "Delaunay Partitioning in Three dimensions and Semiconductor Models" *COMPEL - The INT. J. for Comp. and Math. in IEEE*, 5 pp.75-93 (1986).

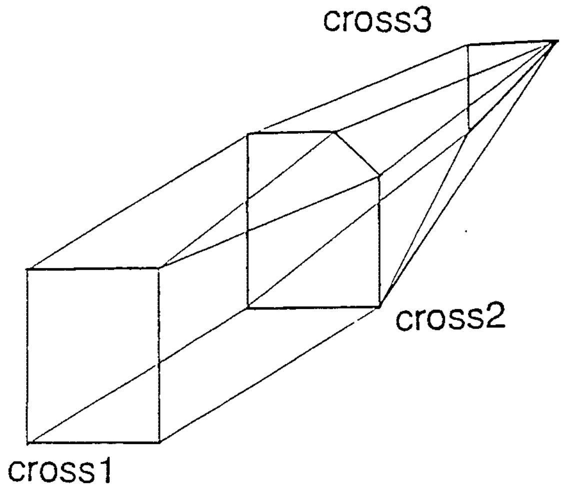

Fig.1 Example of the input process of the 3d-device shape.

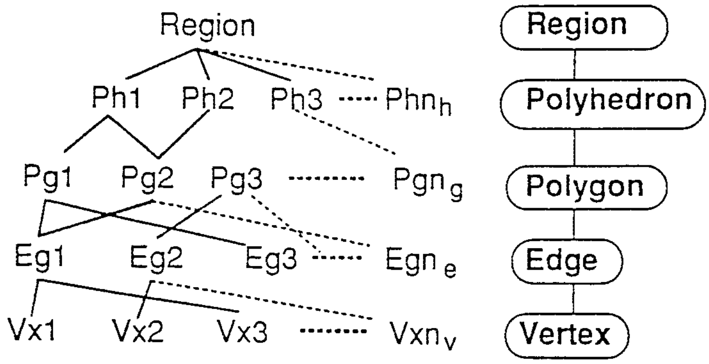

Fig.2 Data structure for 3d-device shape description.

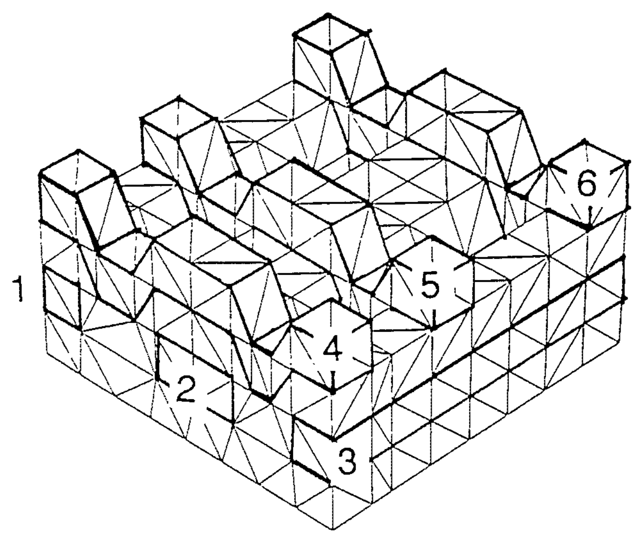

Fig.3 Example of the partitioning.

Table.1 Calculated capacitance matrix of the wired capacitance.
The integer with parenthesis corresponds to the biased electrode and the others, grounded electrodes in Fig.3.

1)-	1--->	-2.8832156458D-15
1)-	2--->	1.0919360322D-15
1)-	3--->	1.5281434465D-20
1)-	4--->	4.4002931882D-16
1)-	5--->	8.3396603124D-16
1)-	6--->	4.5729467741D-16
2)-	1--->	1.0919360322D-15
2)-	2--->	-6.0907773340D-15
2)-	3--->	8.1909730688D-16
2)-	4--->	7.9786847249D-16
2)-	5--->	1.5216879896D-15
2)-	6--->	8.4832949460D-16
3)-	1--->	1.5281430711D-20
3)-	2--->	8.1909730687D-16
3)-	3--->	-3.4406855280D-15
3)-	4--->	4.1830506854D-16
3)-	5--->	7.9028421909D-16
3)-	6--->	4.4610634233D-16
4)-	1--->	4.4002931882D-16
4)-	2--->	7.9786847249D-16
4)-	3--->	4.1830506854D-16
4)-	4--->	-1.7544066129D-15
4)-	5--->	9.8203753007D-17
4)-	6--->	0.0000000000D+00
5)-	1--->	8.3396603124D-16
5)-	2--->	1.5216879896D-15
5)-	3--->	7.9028421909D-16
5)-	4--->	9.8203753006D-17
5)-	5--->	-3.2705726455D-15
5)-	6--->	2.6430652600D-17
6)-	1--->	4.5729467741D-16
6)-	2--->	8.4832949460D-16
6)-	3--->	4.4610634233D-16
6)-	4--->	0.0000000000D+00
6)-	5--->	2.6430652600D-17
6)-	6--->	-1.7781611669D-15