Discretization Problem in Device Simulation for MOSFETs
- The Influence of Grid Size near the Si/SiO_2 Interface on Simulated MOSFET Characteristics -

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1. Introduction

There have been few works on the discretization error caused by an inadequate grid size near the Si/SiO_2 interface for MOSFET simulation. In this work, the discretization problem in device simulation for MOSFETs is discussed using a one-dimensional simulator. We also propose a method to estimate the discretization error.

2. Discretization Schemes and Simulated Results

Figure 1 shows one-dimensional grids for a conventional Delaunay discretization scheme (DD) and for a Voronoi discretization scheme (VD) which is geometrically complementary to DD [1,2].

Figure 2 shows the simulated inversion electron density N_{inv} for MOSFET which has a uniformly doped substrate. The grids are generated uniformly in the Si substrate. For a fine grid, there is a negligible difference between DD and VD. For a coarse grid, there is a discretization error. In the subthreshold region (low V_G), DD results in a larger N_{inv} for the coarse grid and VD reveals a smaller N_{inv}. In the strong inversion region (high V_G), the error in N_{inv} for the coarse grid becomes small for DD. For VD, however, the error in N_{inv} still remains even in the strong inversion region.

3. Subthreshold Region

The discretization error in N_{inv} in the subthreshold region is caused by the numerical integration error in the inversion electron density. As shown in Fig. 3, DD for the coarse grid overestimates N_{inv} and VD underestimates N_{inv}.

We present equations to estimate the discretization error. The electric potential in the subthreshold region does not depend on the grid size, since the inversion carrier density is much smaller than the substrate impurity concentration N_A. Hence, an exact inversion electron density N_{inv}^* can be estimated by depletion approximation.

$$N_{inv}^* = \sqrt{2}\, L_D \frac{n_i^2}{N_A} f(A) \tag{1}$$

where

$$f(A) = \int_0^A \exp(x^2)\, dx \quad , \quad A = \left[2 \log \frac{N_A}{n_i}\right]^{1/2} \quad \text{and} \quad L_D = \left[\frac{kT}{q}\frac{\varepsilon_S}{qN_A}\right]^{1/2} . \tag{2}$$

The numerical integration error is mainly induced at the nearest control volume to the Si/SiO_2 interface, as shown in Fig. 3. The N_{inv} for the coarse grid is approximated by summing up the electron density at the nearest control volume to the Si/SiO_2 interface, and the analytic integration of the electron density in the remaining region. Hence, N_{inv} for DD and VD can be expressed as

$$N_{inv}^D = \frac{\Delta x}{2} N_A + \sqrt{2}\, L_D \frac{n_i^2}{N_A}\, f\left[A - \frac{\Delta x/2}{\sqrt{2}\, L_D}\right] \tag{3}$$

and

$$N_{inv}^V = \Delta x \,\frac{n_i^2}{N_A} \exp\left[\frac{x_d - \Delta x/2}{\sqrt{2}\, L_D}\right]^2 + \sqrt{2}\, L_D \frac{n_i^2}{N_A}\, f\left[A - \frac{\Delta x}{\sqrt{2}\, L_D}\right] \tag{4}$$

where x_d is the depletion width given by

$$x_d = \left[\frac{4\varepsilon_S \phi_F}{qN_A}\right]^{1/2} . \tag{5}$$

The discretization error in N_{inv} can be estimated by N_{inv}^D / N_{inv}^* and N_{inv}^V / N_{inv}^*. Figure 4 shows the simulated N_{inv} and the estimated values using these ratios. This figure reveals the accuracy of the proposed error estimating equations.

4. Strong Inversion Region

Figure 5 shows the simulated gate-channel capacitance C_{GC} ($\equiv q\ \partial N_{inv} / \partial V_G$).

In the case of DD, there is a discretization error in C_{GC} in the subthreshold region. On the other hand, C_{GC} in the strong inversion region scarcely depends on the grid size, and is nearly equal to the gate oxide capacitance C_{ox}. N_{inv} is given by $q^{-1}\int C_{GC} dV_G$, so that the discretization error in N_{inv} is originated from the difference in C_{GC} in the subthreshold region. Hence, the error in N_{inv} for DD in the strong inversion region becomes smaller with an increase in V_G.

On the contrary, C_{GC} for VD is less than C_{ox} even in the strong inversion region. Hence, N_{inv} is small even in the

strong inversion region , as shown in Fig. 2. ${C_{GC}}^V$ can be derived as

$$\left[{C_{GC}}^V\right]^{-1} = \left[C_{ox}\right]^{-1} + \left[\frac{\varepsilon_S}{\Delta x/2}\right]^{-1} . \tag{6}$$

Equation (6) means that C_{GC} for VD contains a quasi capacitance which is equal to $\Delta x/2$ thick Si. This is the reason why VD underestimates N_{inv} in the strong inversion region. Equation (6) indicates that ${C_{GC}}^V$ is nearly equal to C_{ox} for a fine grid.

References

[1] Y. Saito *et al.*,"Faster Magnetic Field Computation Using Locally Orthogonal Discretization," IEEE Trans. Magn., MAG-22, p.1057, 1986.

[2] T. Kojima *et al.*,"A Proposed Semiconductor Device Simulator Using a Voronoi Mesh System," IEICE Tech. Report, SDM89-103, p.13, 1989 (in Japanese).

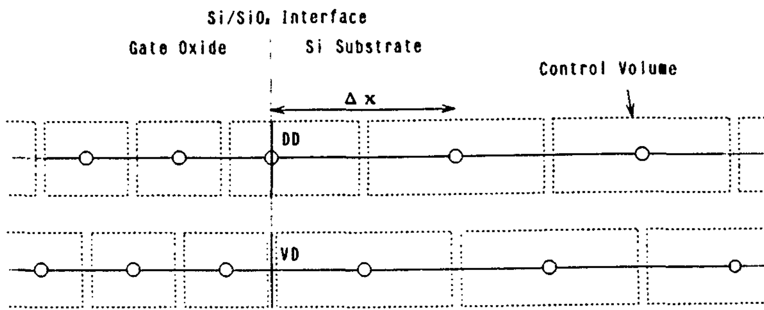

Fig. 1 One-dimensional grid for Delaunay discretization scheme (DD) and Voronoi discretization scheme (VD).

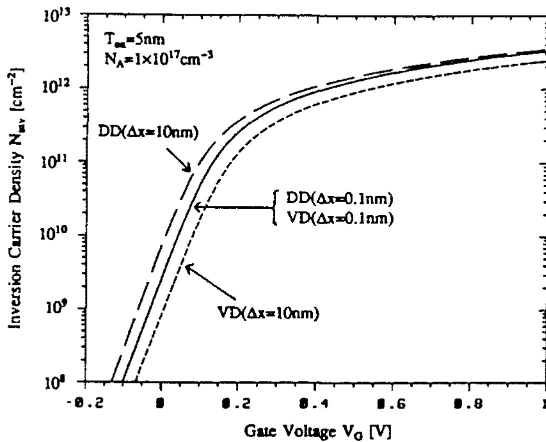

Fig. 2 Dependence of simulated inversion electron density on grid size for DD and VD.

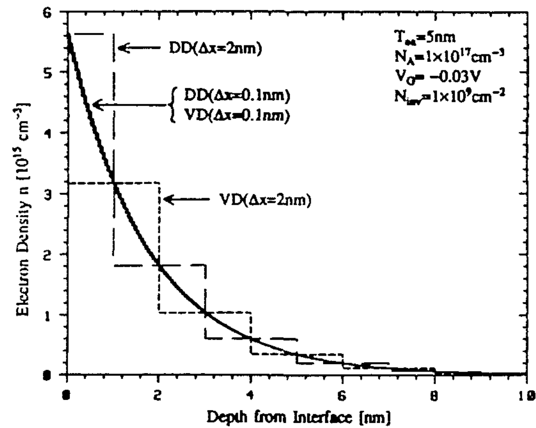

Fig. 3 Simulated inversion carrier density profiles in subthreshold region.

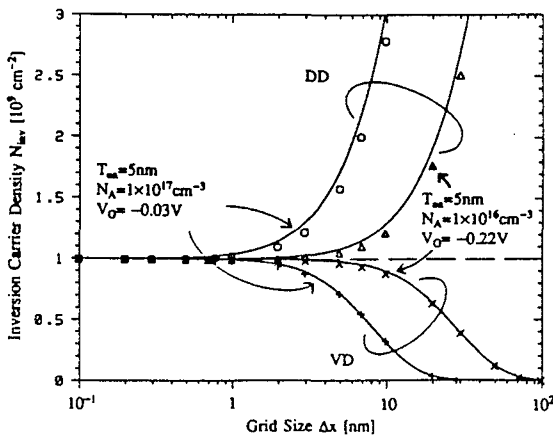

Fig. 4 Simulated inversion electron density for different grid sizes and substrate concentrations in the subthreshold region. Solid lines are estimated values using equations (1), (3) and (4).

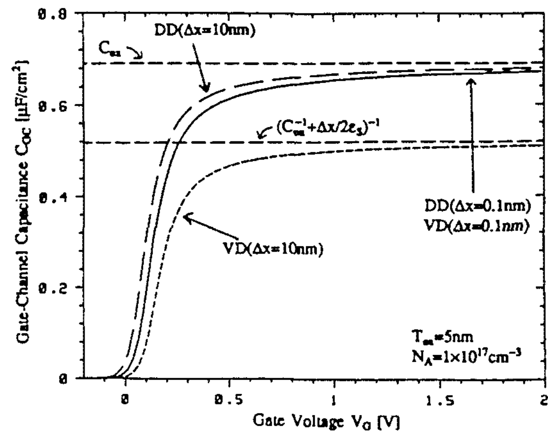

Fig. 5 Simulated gate-channel capacitances in the strong inversion region. C_{ox} and $(C_{ox}^{-1}+\Delta x/2\varepsilon_S)^{-1}$ are also shown.