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MODELING OF INTERCONNECT CAPACITANCE OF MULTIPLE CONDUCTOR PACKAGE BY STATISTICAL CENTRAL COMPOSITE DESIGN FOR VLSI STRUCTURES

BY

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The influence of parasitic effects on the performance of VLSI circuits can be improved by reducing the interconnect capacitance and resistance. In high speed bipolar VLSI circuits, delay through the metal interconnect has become an important design consideration. The average interconnect length grows with increasing circuit complexity and chip area, making the consideration of parasitic effects a necessity in order to accurately simulate the VLSI circuit performance. Although numerical simulators are extremely powerful in the analysis of parasitic capacitance, due to the large amount of data that has to be manipulated in VLSI circuit simulation, single closed form analytical formulas are desired.

The parasitic capacitance problem is three dimensional by nature and described by three distinct capacitance components; metal line to ground, metal to metal line, and cross over between metal lines on different layers. All these parasitic components are significant for VLSI circuit performance where the interconnection pitch is approaching less than three microns.The non linear behavior of MLM parasitic capacitance can be optimized by statistical methodology taking into account multiple process variables as inputs. Central Composite Design (CCD) is used to obtain the closed form expression for parasitic capacitance as a function of five process variables; metal thickness, interlayer dielectric thicknesses, metal width, and metal space.The closed form solutions are compared with numerical solutions for MLM- VLSI structures.

The calculation of capacitance from simple parallel plate approximation to complex numerical calculation is described in references [1] to [3]. The statistically derived analytical expression for capacitance discussed here is easy to use and reasonably accurate for small pitch multi layer conductor VLSI circuits. The CCD [4] is to fit a non linear model (second order polynomial) to a response parameter 'R' as a function of controlled input factors X1,X2,X3.... The input factors are at five levels and the design consists of factorial points, center point, and axial (star) point. The response as a function of five input factors can be written mathematically as

$$R=bo+b1X1+b2X2+b3X3+b4X4+b5X5+b6X1^2+b7X2^2+b8X3^2+b9X4^2+b10X5^2+b11X1X2$$
$$b12X1X3+b13X1X4+b14X1X5+b16X2X3+b17X2X4+b18X2X5+b19X3X4$$
$$b20X3X5+b21X4X5$$

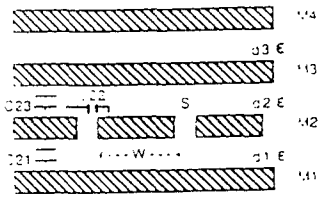
where X1,X2,X3,X4, and X5 are continuous or discrete process input factors and the coefficients b0,b1,b2..... are constants. In our design the response is the parasitic capacitance and the process factors to be assigned to X1,X2,X3,X4, and X5 are metal space (S), metal width (W), metal thickness (TM),dielectric layer-1 thickness (d1), and dielectric layer-2 thickness (d2) as shown in fig 1. The second and third metal layers are orthogonal and assumed to be signal lines. The analytical expression should give the various capacitance components and the total capacitance seen by a metal layer (example metal 2 as in fig 1) due to interactions among all metal layers. The five levels assigned for each process factor for the CCD design is shown in Table 1. The CCD design was repeated for very small metal width with X2 input variable at a different level.

PISCES [5] and PCMOM [6] are used to simulate MLM structures to calculate total parasitic capacitance for the above statistical design.The pisces solution ,the internal distribution of potential and electric field at a specified bias and the total parasitic capacitance for different bias conditions for one of the MLM conditions in table 1 are shown in fig 2 . PCMOM , a numerical simulator uses the method of moments to solve Laplace equation for evaluating parasitic capacitance for MLM structures and a sample of output capacitance matrix is shown in table 2 for one of the MLM conditions as defined in table 1.The parasitic capacitance simulation results from PISCES and PCMOM agree very well and PCMOM is used in this statistical CCD work for deriving analytical expression .

The five factor, twenty seven run, five level split matrix was run using PCMOM and the capacitance result is fitted to a second order polynomial using multiple regression analysis. The significant input variables are identified from 't' statistics and the compact analytical expression derived by choosing statistically significant input factors is shown in table 3. It is important to remember that these equations are valid within the boundary defined by CCD for the five input factors. It is easy to define CCD methodology with a new set of boundary conditions for the process input factors to suit the needs of MLM to derive the closed form solution.

The parasitic capacitance expression is non linear with square terms and interaction terms among input process factors as shown in table 3. As an example, Fig 3 shows the comparison of total capacitance versus metal pitch for PISCES, PCMOM, and the analytical expression derived from CCD for a given metal space. The analytical fit is excellent to within 5% of the results from PISCES. Fig 4 shows the 1Pf equivalent interconnect length versus metal pitch for a fixed metal width as a figure of merit derived from the analytical expression. It is easy to generate plots using the analytical expression for different conditions of process input factors. The results clearly shows the complex nature of the capacitance behavior with respect to process input factors and the importance of fringe capacitance contribution to the overall total capacitance. The analytical expression also allows one to calculate the resistance of the metal lines and RC time delay as a figure of merit (lumped) for different MLM geometries.

Multilevel metallization parasitic capacitance was presented for VLSI structures. The analytical expression for estimating various capacitance components is derived using central composite statistical design.The closed form solution is derived using PCMOM and compared with PISCES.The agreement is excellent to within 5% for advanced MLM geometries. Finally the comparison of measured capacitance results to the derived capacitance from analytical expression will be discussed.



CTOT= C23+C21+2 C22

FIG 1 CROSS SECTION OF FOUR LEVEL MLM STRUCTURE

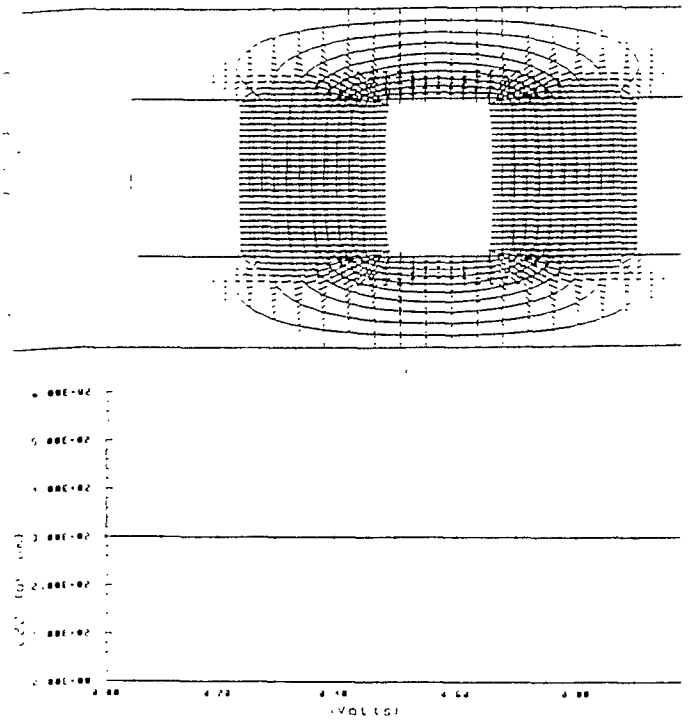


FIG 2 A SAMPLE OF PISCES OUTPUT a) POTENTIAL AND ELECTRIC FIELD DISTRIBUTION b) TOTAL PARASITIC CAPACITANCE VERSUS VOLTAGE

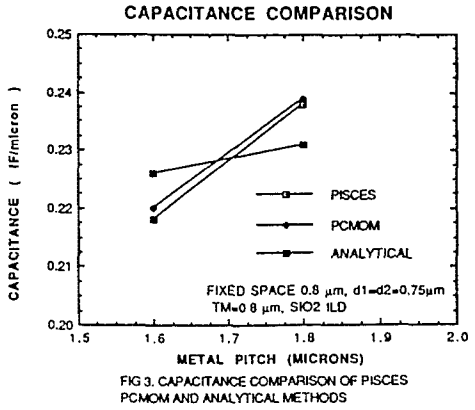


FIG 3. CAPACITANCE COMPARISON OF PISCES PCMOM AND ANALYTICAL METHODS

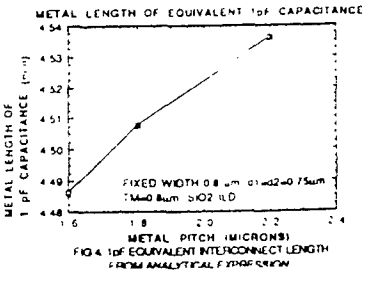


FIG 4. 1pF EQUIVALENT INTERCONNECT LENGTH FROM ANALYTICAL EXPRESSION

PROCESS INPUT FACTORS(MICRONS)	LEVELS -2	-1	0	+1	+2
X1 (METAL SPACE)	0.6	0.8	1	1.2	1.4
X2 (METAL WIDTH)	0.6	0.8	1	1.2	1.4
X3 (METAL THICKNESS)	0.6	0.7	0.8	0.9	1
X4 (DIELECTRIC-1 THICKNESS)	0.6	0.7	0.8	0.9	1
X5 (DIELECTRIC-2 THICKNESS)	0.6	0.7	0.8	0.9	1
X2 (METAL WIDTH)	0.1	0.2	0.3	0.4	0.5

TABLE 1 CCD DESIGN LEVELS FOR FIVE MLM PROCESS INPUT FACTORS

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GEOMETRY OPTION                    :  TWO GROUND PLANES (ONE AT Y=0)

NUMBER OF ACTIVE CONDUCTORS        :  3

NUMBER OF GROUNDED CONDUCTORS      :  2

NUMBER OF DIELECTRIC INTERFACES    :  0

NUMBER OF SUBINTERVALS/SIDE        :  5

MAX. EXTENT OF DIEL. DISCRETIZATION :    7.000

DIELECTRIC DATA:
 REGION #  1 REAL EPSILON =   3.9000   LOSS TANGENT =   0.0000

CONDUCTOR DATA:
ACTIVE CONDUCTOR #   VERTEX #    (X,Y) COORDINATE
          1              1        2.000     0.900
          1              2        2.200     0.900
          1              3        2.200     1.600
          1              4        2.000     1.600
          2              1        1.000     0.900
          2              2        1.200     0.900
          2              3        1.200     1.600
          2              4        1.000     1.600
          3              1        3.000     0.900
          3              2        3.200     0.900
          3              3        3.200     1.600
          3              4        3.000     1.600

GROUND CONDUCTOR #   VERTEX #    (X,Y) COORDINATE
          4              1        0.000     0.900
          4              2        0.200     0.900
          4              3        0.200     1.600
          4              4        0.000     1.600
          5              1        4.000     0.900
          5              2        4.200     0.900
          5              3        4.200     1.600
          5              4        4.000     1.600

ARBITRARY GROUND PLANE POSITION =    2.300

PARAMETER CALCULATOR RESULTS:

CAPACITANCE MATRIX (pf/cm)

          1           2           3
1      1.49542    -0.32152    -0.32152
2     -0.32152     1.41862     0.03264
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TABLE 2. A SAMPLE OF PCMOM OUTPUT CAPACITANCE MATRIX RESULT

C TOT = 0.2244-0 00842 X1+0 0185 X2+0.00725 X3-0.00642 X4-0.00817 X5
+0.00255 X1^2-0.00138 X1X3-0.00137 X2X5

C22 = 0.0187-0.01079 X1-0.00229 X2+0.00337 X3+0.00104 X4+0.00413 X5
+0.002 X1^2-0 0081 X1X3

C23 +C21 = 0.18315+0 01325 X1+0.02317 X2-0 00892 X4-0.01625 X5
-0 00094X1^2+0.00106 X4^2+0.00243 X5^2-0.001 X1X5
-0 001 X2X4-0.00237 X2X5

TABLE 3. ANALYTICAL EXPRESSION OF CAPACITANCE COMPONENTS FOR WIDER METAL WIDTH (0 6- 1.0 MICRONS) MLM STRUCTURE

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