(9A-6)

Evaluation of Circuit Reduction for Pattern Based Circuit Simulation

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Introduction

With the increase in VLSI performance, precise performance analysis of the LSI has been required including that of its parasitic elements, such as resistance and capacitance, which are extracted directly from the layout pattern data. As the complexity of the LSI increases, the number of elements extracted also increases. Therefore, cost effective simulation of the entire circuit has been impossible using a conventional circuit simulator.

This paper proposes a new method to reduce the simulation size of the circuit, by extracting the specified critical path out of the entire circuit, and then reducing the parasitic elements. This method is implemented in the circuit extractor HICE (Hierarchical Circuit Extraction System)[1][2][4].

Circuit Extractor HICE

HICE consists of four subsystem as shown in Figure 1. The transistor level circuit is first reconstructed from the layout pattern data. Next, in the recognition subsystem, the elements that consist logic gates, such as inverters and NAND gates are combined into groups, and then directions of the signal flow among the gates are determined. Then in the reduction subsystem, specified critical paths are extracted from the transistor level circuit data, and parasitic elements are reduced. In the final subsystem, the net list for the circuit simulation is created.

The algorithm of the reduction subsystem and some evaluation results will be described.

Circuit Reduction

In this circuit extractor (Fig 1.), the size of the circuit will be reduced in two steps.

First, as shown in Figure 2, by specifying the input and the output of the critical path, all of the gates which are included in the path are automatically selected by tracing the signal flow, and the selected part will be extracted from the entire circuit. The elements connected between the extracted circuit and the eliminated circuit are changed to capacitive loads to retain accuracy.

After the critical paths have been extracted, the parasitic elements are combined or deleted according to the tolerance error which is specified by the user. Parasitic elements on the signal bus are combined or deleted if the estimated error of the RC time constant[3] after reduction differs from the one before reduction by not more than the tolerance error (Fig 3). On the other hand, parasitic elements on the power bus are combined or deleted from the circuit depending on the IR-drop of the DC characteristics (Fig 4).

Evaluation Results

Table 1 shows our evaluation results of circuit reduction efficiency. Benchmark circuits are control circuits of memory cells and logic macrocells. The number of elements is reduced to 1/17-1/48 as compared to the number of the elements before reduction.

Reference

[1] G. Yokomizo, et al., "HICE: Hierarchical Circuit Extraction System for Layout Verification," Proc. CICC-87, pp.133-136, 1987.
[2] G. Yokomizo, et al., "A Circuit Reduction Method for Pattern Based Circuit Simulation," Proc. CICC-90, pp.9.4.1-9.4.4, 1990.
[3] P. Penfield, Jr., "Signal delay in RC tree networks," Proc. 18th-DAC, pp.613-617, 1981.
[4] M.Miyama, et al., "Method of Critical Path Extraction in HICE System," IPSJ-90, pp.132, 1990.

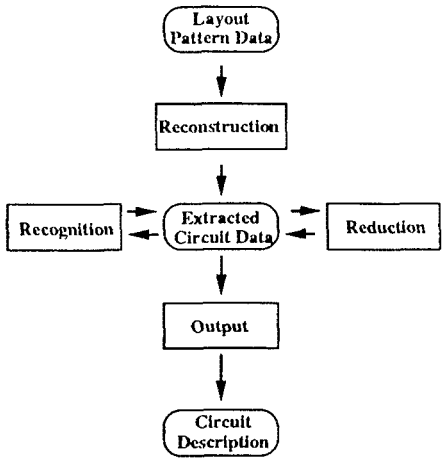


Figure 1. System configuration of HICE

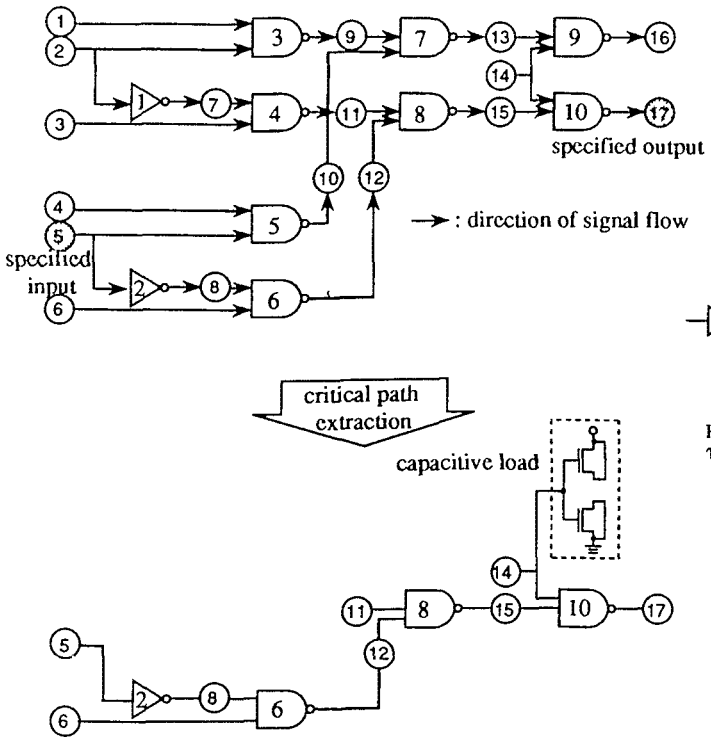
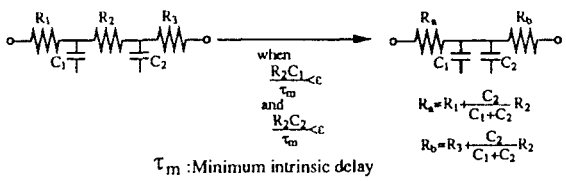


Figure 2. Critical Path Extraction

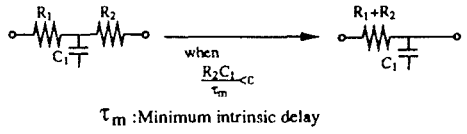
Table 1. Evaluation Results

	Number of elements		(b)/(a)
	before reduction (a)	after reduction (b)	
Control circuit of memory cell(a)	788,631 (15,607)	33,185 (5,035)	1/24
Control circuit of memory cell(b)	490,101 (8,479)	14,905 (2,430)	1/33
Logic macrocell(c)	280,757 (8,277)	16,246 (2,759)	1/17
Logic macrocell(d)	157,967 (5,409)	3,284 (602)	1/48

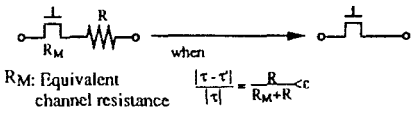
( ) number of MOS transistors included in the circuit



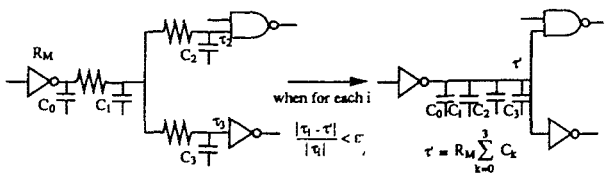
(a) Combination of three series signal resistors



(b) Combination of two series signal resistors

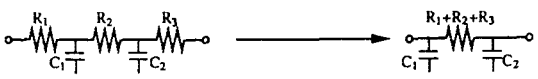


(c) Elimination of a source resistor

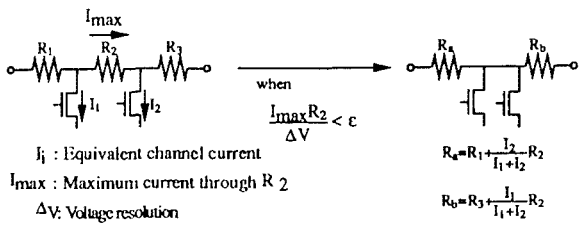


(d) Elimination of signal resistors

Figure 3. Parasitics Reduction Methods for Signal Nets



(a) Combination of series power resistors



(b) Combination of three series power resistors

Figure 4. Parasitics Reduction Methods on Power Bus Nets