A Modular Approach to Parallel Mixed Level Device/Circuit Simulation

B. Meinerzhagen, J.M.J. Krücken, K.H. Bach, F.M. Stecher and W.L. Engl

Institut für Theoretische Elektrotechnik, University of Aachen
Kopernikusstr. 16, D-5100 Aachen, West-Germany

In mixed level device/circuit simulation (MLDCS) semiconductor devices are modeled by partial differential equations (e.g. the drift diffusion model) while being embedded in a realistic circuit environment named carrier network [1]. For each DC bias or point in time the mixed level device/circuit simulator alternates between device and circuit level until convergence is reached. At the device level the small signal admittance matrix and the terminal currents are evaluated based on the underlying partial differential equations for each embedded device and the given bias conditions at the device terminals. At the circuit level the linearized carrier network equations supplemented by the small signal admittance description of the embedded devices are solved leading to an update of the voltages at the device terminals.

In order to see how MLDCS can be performed efficiently one has to recollect the following facts:

A) The device level is by far the most time consuming part. On the other hand the small signal admittance matrices can be computed in parallel.

B) The amount of information to be transferred between the device and circuit level and vice versa is very limited and depends only on the number of embedded devices and device terminals connected with the carrier network. Moreover at the device level no information is transferred between different devices.

A) implies that MLDCS is a good candidate to be efficiently implemented on parallel architectures, whereas B) implies that there is no need for high speed communication channels to and from the different processors.

Hence a cluster of independent workstations coupled by a local area network (LAN) should be sufficient to run MLDCS efficiently in parallel. In fact for workstation clusters coupled by ethernet and running under UNIX – which is already a common configuration in industry – a parallel implementation of MLDCS is feasible, since the socket based interprocess communication under UNIX allows to control parallel processing on such architectures. The modular nature of MLDCS – the circuit level collecting the device information from the various device simulations at the device level – directly maps to the client/server process model, on which modern UNIX networking tools like e.g. X-Windows are based. In case of MLDCS the client can be identified with the circuit level and the server with the device level, respectively.

By exploiting the simulators MEDUSA [1] and GALENE II [2] as modules for circuit and device level, respectively, a client/server system has been established being capable of performing MLDCS in parallel on LAN's in an UNIX environment. A brief description of this system can be seen in fig.1. Parallel MLDCS is initialized by starting MEDUSA acting as client on one of the workstations. Via the socket base interprocess communication facilities the MEDUSA client establishes a bidirectional communication channel to the GALENE II servers, which are small size processes permanently residing on all workstations of the cluster. Via these channels the necessary information like bias conditions and small signal admittance matrices is transferred to and from the GALENE II servers, respectively. Moreover the GALENE II servers control the device simulations performed by GALENE II on the different workstations of the cluster.

In order to demonstrate the efficiency of this approach the DC transfer characteristic (see fig. 3) of the ECL-gate shown in fig.2 has been simulated by the above described system. Within this circuit, device level simulations have been performed with GALENE II for all four bipolar transistors. Three different clusters consisting of one, two and four MIPS workstation were chosen to run MLDCS for this circuit. Table 1 gives an overview over the total calculation time used and the efficiency of the parallelization on the different unloaded clusters. As can bee seen, a speed up of about three is achieved if four workstations are used, which clearly demonstrates the usefulness of this approach.

References

[1] W.L. Engl, R. Laur and H.K. Dirks:"MEDUSA – A Simulator for Modular Circuits:, IEEE Trans. on CAD, Vol. CAD-1, 1982, pp. 85 - 93.

[2] K.H. Bach, H.K. Dirks, B. Meinerzhagen and W.L. Engl:" Nonlinear Variable Transformation for Improved Convergence of Gummel's Relaxation Scheme", NUPAD III Digest of Technical Papers, 1990

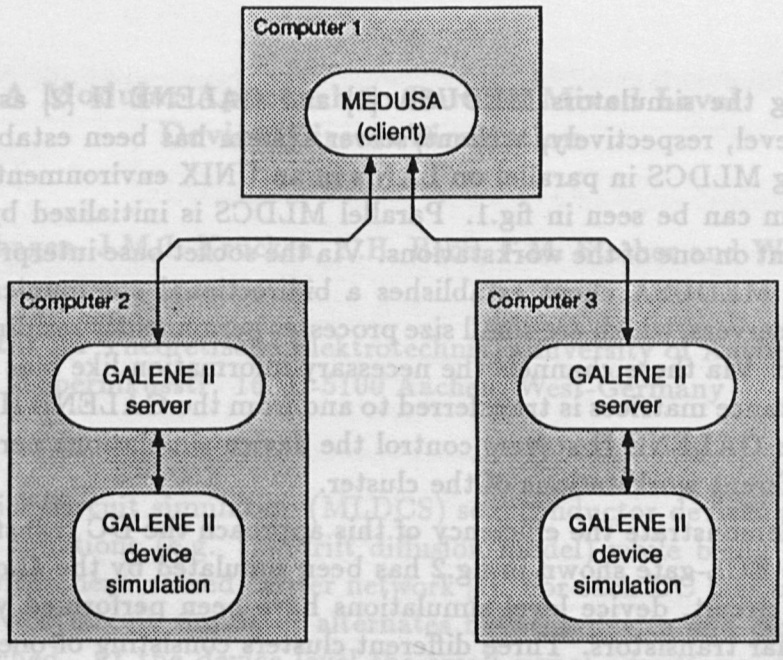

Fig. 1: MEDUSA/GALENE II Client/Server system for MLDCS

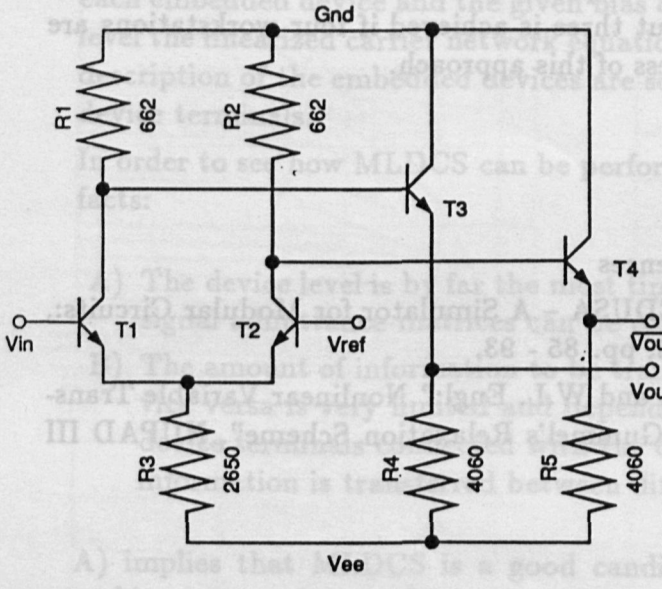

Fig. 2: Example ECL- Circuit

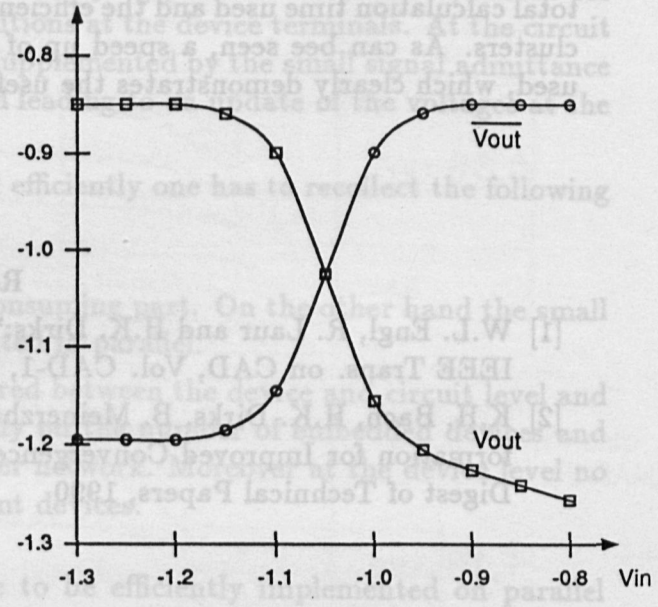

Fig. 3: DC Transfer Characteristic simulated by parallel MLDCS

# of workstations	Calculation time (min)	Speedup	efficiency
1	183	1	1
2	102	1.80	0.9
4	62	2.95	0.74

Tab. 1: Total calculation times, Efficiency on unloaded clusters