# [INVITED] MOSFET Modeling for VLSI Circuit Simulation

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## 1. Introduction

In the VLSI era, the role of circuit simulation becomes increasingly important for designing very large-scale and high-speed circuitry. This paper surveys VLSI circuit simulation problems.[1] In particular, how an MOSFET model is affected by sub-micron sizes, [2] and temperature dependency [3] of its I-V and CV characteristics will be examined.

## 2. VLSI Simulation

Recent VLSI trends towards high integration, miniaturization of MOSFETs, and high speed have created a number of requirements for MOSFET device modeling and circuit design, as shown in Table 1. (1) Scaled-down devices and processes to the submicron level cause capacitive coupling between signal lines and cause the short & narrow channel effect in MOSFETs.[4-6] (2) A highly integrated circuit has an additional problem of mutual-interference among sub-circuits on a chip, thereby requiring large-scale circuit-level chip simulation. (3) High-speed transitions of input and internal pulses require precise circuit simulation, which includes the inductance of lead wires and package pins, and the transmission line effect of signal lines and active devices (non-quasi-static mode operation [7-8] ). Figure 1 shows the result of three-dimensional capacitance simulation result of a dynamic memory cell. Here, the inter-pair capacitive coupling of data lines becomes significant in lines of less than a 4-μm pitch.[9] Circuit extraction and chip simulation of large-scale dynamic memory was also reported as shown in Fig. 2, in which circuit simulation for a few memory cycles required 11 hours of CPU time on a super computer.[10]

## 3. Submicron MOS modeling

Requirements of the circuit model in VLSI simulation are as follows (see Table 2). First, the basic model equation must be simple, to reduce CPU cost and to make circuit operation easy to understand for designers. Thus, the number of model parameters should be minimized. Second, the short channel effect must be accurately formulated in accordance with channel length (L), and the temperature (T) model is also necessary for designing high-speed, high-power VLSIs. Third, the automatic model parameter extraction system is an essential tool for determining the parameters of the circuit model.[11] Besides these three requirements, the I-V model must agree closely with experimental values, that is, it must have an error of less than a few percent. In the following, we will present an example of a submicron MOS model (MOSTSM) having 14 basic parameters, including L and T dependencies in the I-V equation.

### 3.1. MOSTSM Formulation [2-3]

(a) Weak-inversion model

The following I-V model is used to describe MOSFET sub-threshold conduction.

$$I_{ds} = \beta^* * \left(1 - \exp\left(\frac{-V_d}{V_t}\right)\right) \exp\left(\frac{AV_e}{\beta^*}\right) \qquad (1)$$

$$\beta^* = \beta_0 \left(\frac{W}{L}\right) \frac{1}{A} \left(\frac{kT}{q}\right)^2 \qquad (2)$$

where, Vd is drain voltage, Vt threshold voltage, A sub-threshold slope coefficient, Ve effective gate voltage (=Vg - Vt), βo channel conductance of the unit gate area, W and L channel width and length, and (kT/q) the Boltzmann voltage.

(b) Strong-inversion model

We employed the simple I-V equation as shown below for the linear operational region,

$$I_{ds} = \frac{W}{L} \beta_{eff} \left(V_e - \frac{a}{2} V_d\right) V_d \; ; \qquad \text{Linear region} \qquad (3)$$

Here, parameter 'a' exhibits an effective depletion charge effect. We formulate the gate-field effect on 'βeff' as,

$$\beta_e = \frac{\beta_o (\sqrt{\theta_{e1}} + \sqrt{\theta_{e2}})^2 V_e}{(1 + \theta_{e1} V_c)(1 + \theta_{e2} V_e)} \quad (4)$$

where, 'θe1' and 'θe2' indicate high and low gate field factors, respectively. It is noted that the βo is a unique value that is independent of device dimensions L and W (channel width).

(c) Channel length (L) dependency

Based on extensive parametric study of devices, we formulate each model parameters having an L-dependent function. Key parameters of the model have the following formula.

$$V_{to},\ K_b\ (\text{threshold related parameters}) \Rightarrow (1 - \exp(\frac{-L}{L_o})) \quad (5)$$

$$\theta_{e1},\ \theta_{e2}\ (\beta_{eff}\ \text{related parameters}) \Rightarrow L^{\pm n} \quad (6)$$

(d) Temperature (T) dependency

Since βo is the maximum channel conductance (low field carrier mobility), βo shows $T^{-n}$ dependency, which is predicted by carrier transportation physics.[12] However, it was found that the θe1 also shows similar temperature dependency. In the MOSTSM, four model parameters have the following temperature-dependent formulas.

$$V_{to},\ \frac{1}{A} \Rightarrow \text{Const. x } (T - T_o) \quad (7)$$

$$\beta_o,\ \theta_{e1} \Rightarrow \text{Const. x } (\frac{T}{T_o})^n \quad (8)$$

3.2 Experiment

Figure 3 shows an experimental verification of the MOSTSM, using devices fabricated by 0.8 to 2.0-μm CMOS technologies. As shown in the figure, the experimental agreement is excellent with biases of Vg=0 to 5 V and Vd=0 to 5 V. Figure 4 shows an experimental verification of the L- and T-dependent model used in the MOSTSM. MOSFETs fabricated with experimental 0.5-μm CMOS technology are used for the evaluation. The model shows reasonable agreements with the experimental data, demonstrating an RSM error of less than 2%.

In deep-submicron MOS devices, device physics of the quantum effect, hot carrier device degradation,[13] low-temperature operation,[14] and non-quasi static behavior in high-speed, high-frequency operation [7-8], are expected in the future.

## References


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Table 1 Problems and Requirements for VLSI circuit simulation

| TRENDS | CKT DESIGN | MOSFET MODELING |
|---|---|---|
| ( 1 ) SCALED-DOWN | PARASITIC 'C'. AND 'R'. COUPLING 'C'. BETWEEN LINES. | SHORT & NARROW CHANNEL EFFECTS. LDD SERIES RESISTANCE. |
| ( 2 ) HIGH-INTEGRATION | INCREASE OF CPU TIME. NON-CONVERGENCY | CONTINUOUS IN 'G' & 'Q'. MACRO-MODELING |
| ( 3 ) HIGH-SPEED SWITCHING | 'L' OF WIRE & PACKAGE. ELECTRIC AND CURRENT NOISE. | NON-QUASI STATIC BEHAVIOR |

( C: Capacitance, R: Resistance, L: Inductance, G: Conductance, and Q: Charge )

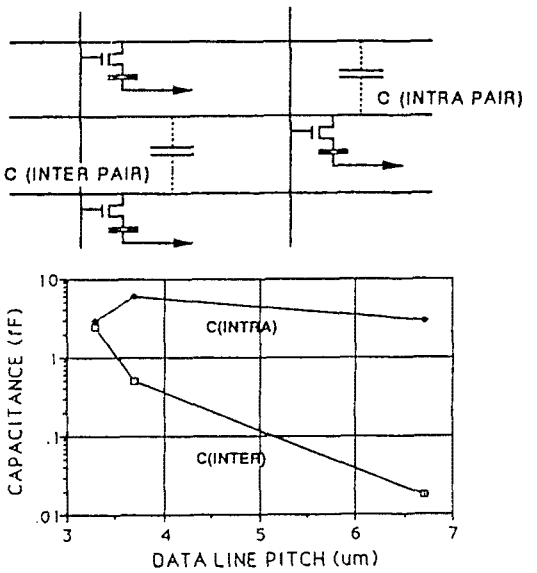
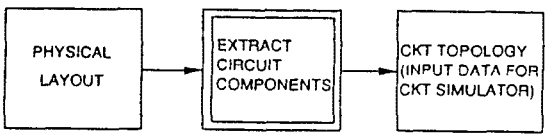



Fig. 1 Three-dimensional simulation of data-line capacitances in DRAM.




(A) CKT COMPONENT EXTRACTION SYSTEM

| COMPONENT | NO OF COMPONENT |
|---|---|
| MOSFET | 10,491 |
| CAPACITOR | 5,925 |
| RESISTOR | 1,807 |

(B) EXTRACTED COMPONENTS BASED ON DRAM CHIP LAYOUT

Fig. 2 Circuit components extraction from chip layout for the chip simulation with a DRAM.

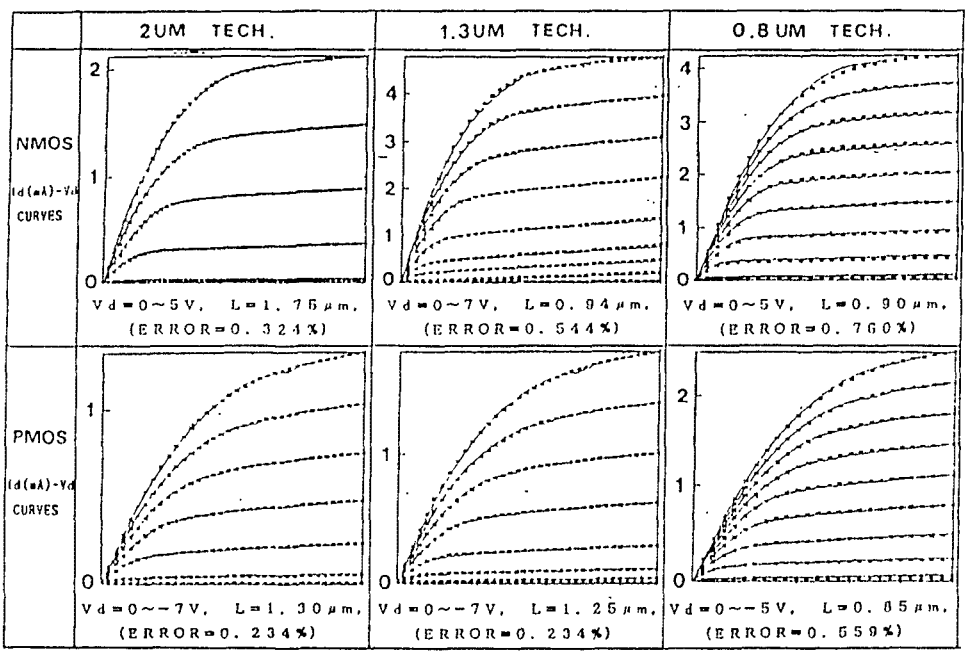



Fig. 3 Comparison of I-V curves between experiments and the MOSTSM model.

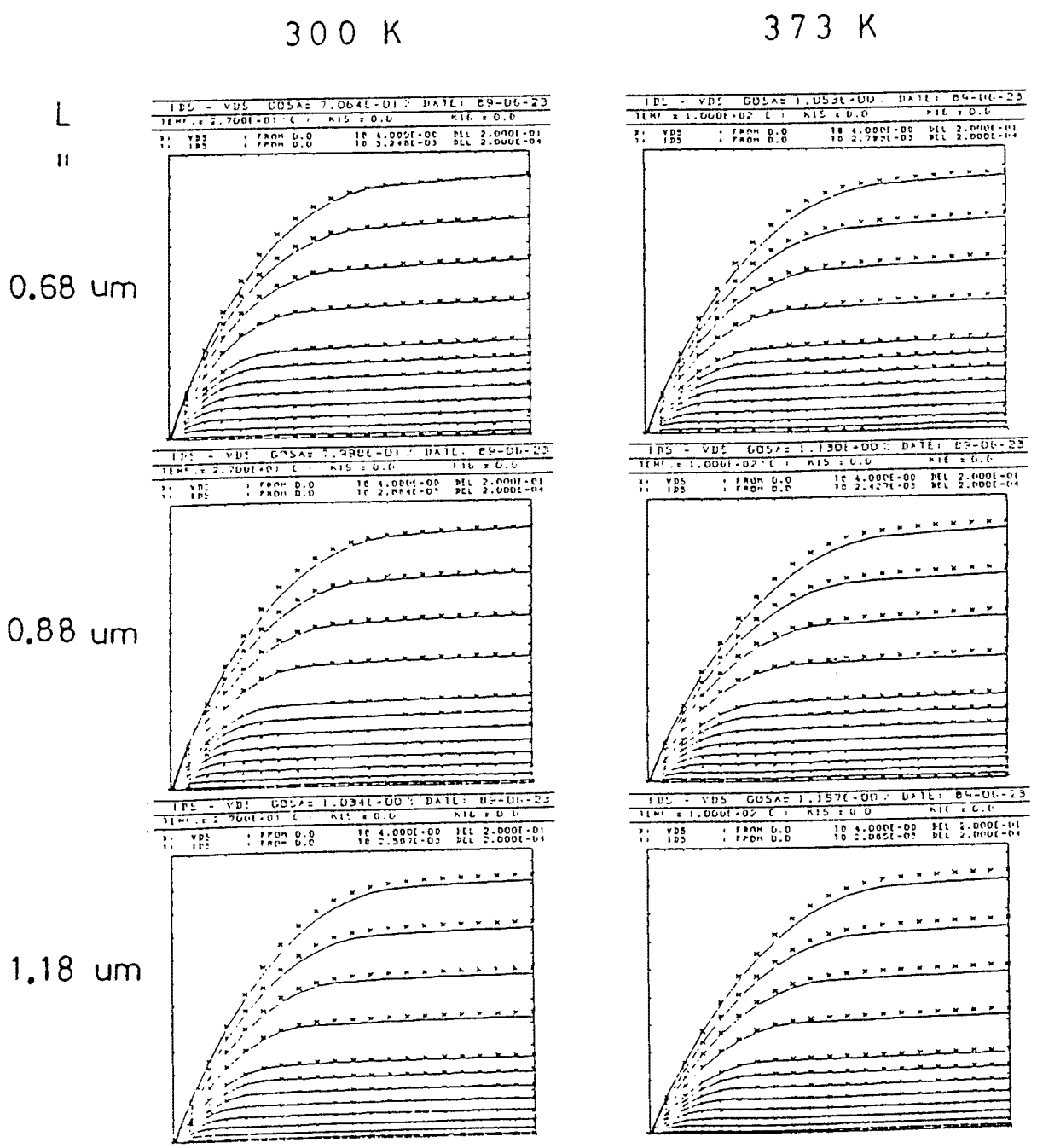



Fig. 4 Experimental velification of channel-length (L) & temperature (T) dependent models in the MOSTSM, using NMOSs fabricated by a 0.5 μm technology.