Electrical Isolation Rule for GaAs IC's Fabricated on LEC Substrates

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Summary

Most present day GaAs digital integrated circuits are fabricated by direct ion implantation into semi-insulating (SI) substrates grown by the liquid-encapsulated Czochralski (LEC) technique. One of the advantages of this approach is that device isolation between active elements can be easily achieved by utilizing the high resistivity ($10^7 \Omega cm$) of the bulk substrate material. This greatly simplifies the fabrication process. As the drive for packaging more functions on the chip continues, device sizes are constantly reduced and isolation spacings decreased. Accompanying this trend are short-channel effects and an increase of leakage current between two active devices. This places an upper limit on the circuit density that can be achieved. A careful examination shows that both effects are related to the electrical properties of parasitic N-Semi-insulating(SI)-N triple-layer structures as indicated in Fig. 1. Therefore the study of the behavior of N-SI-N structures is very important for the design of reliable integrated circuits.

To rigorously investigate the electrical properties of N-SI-N structures, a two-dimensional device simulator was developed [1]. In order to account for the semi-insulating properties of LEC substrates, a deep donor compensation model was incorporated [2]. Figure 2 shows the I-V characteristics of N-SI-N structures calculated by this device simulator. As can be seen from the figure, the current flow through the structure is characterized by a slowly varying region followed by a sharply increasing region. This characteristic can be explained by a barrier lowering effect caused by the punch-through phenomenon. Before punch-through, the anode N-SI junction is separated from the cathode N-SI junction by a neutral SI layer and thus the I-V curve shows a linear relationship with a very small proportionality which characterizes the neutral SI layer. As the applied voltage increases, the edge of the space charge region of the anode approaches that of the cathode. Eventually the neutral SI layer is completely depleted. After that, the cathode N-SI junction potential barrier will be decreased by the anode voltage. Therefore, according to Boltzmann statistics, the number of electron that overcome the cathode potential barrier is increased by an exponential factor whose index is proportional to the amount of the potential lowering. As a result, the current increases sharply. To illustrate the punch-through phenomenon, Fig. 3 shows the three-dimensional plot of the energy band structure corresponding to an anode bias voltage of 2.5V (which is close to the onset of the punch-through condition of this structure) for an N-SI-N structure with a SI layer thickness of $3\mu m$. Although two-dimensional simulation can provide detailed device operating information, it is relatively expensive to apply. To facilitate the development of design rules for device isolation, it is very helpful to develop a simplified model for the punch-through voltage. Such a model has been derived by utilizing cylindrical coordinates and abrupt transition region assumption. Based on this derivation, we can obtain the punch-through voltage as a function of the length of the SI layer using the residual acceptor concentration as a parameter. Such a graph is shown in Fig. 4. In the calculation, the deep level concentration is assumed to be larger than the residual acceptor concentration by an order of magnitude. With the help of this diagram, a quick estimation of a safe spacing between active devices for an electrical isolation design rule development can be obtained.

References:

1. Jyh-Chwen Lee, Ph.D. Thesis, Carnegie Mellon University (1990).

2. G. M. Martin, J. P. Farges, G. Jacob, J. P. Hallais, and G. Poiblaud, J. Appl. Phys., 51(5), 2840-2852(1980).

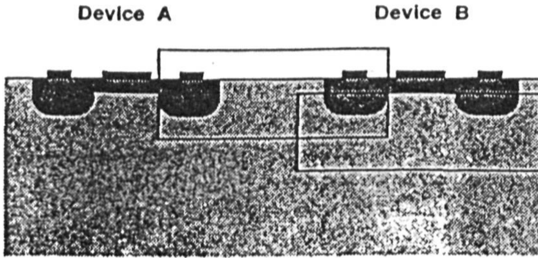

Figure 1: Two typical parasitic N-SI-N structures of a self-aligned GaAs IC.

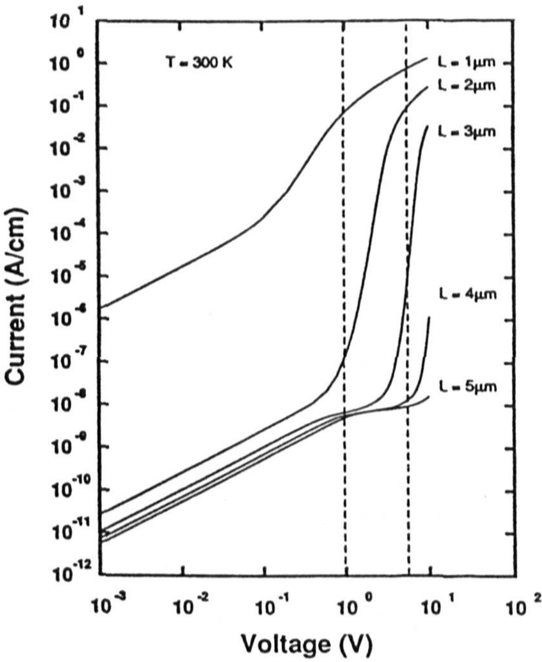

Figure 2: I-V characteristics of N-SI-N structures calculated by a two-dimensional device simulator. The energy level of the deep donor is $0.69eV$ and the concentration is $10^{16}cm^{-3}$. The residual acceptor concentration is assumed to be $10^{15}cm^{-3}$. Dashed lines indicate punch-through voltages corresponding to L = $2\mu m$ and L = $3\mu m$ calculated by analytical expressions.

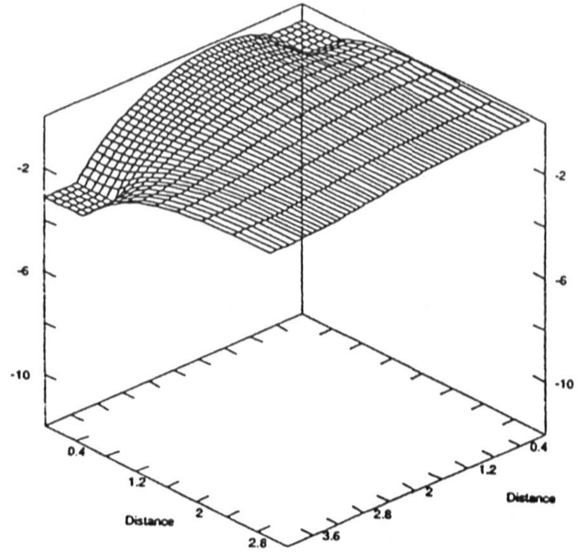

Figure 3: Three-dimensional perspective of the energy band corresponding to an anode bias voltage of 2.5V for the N-SI-N structure with a SI layer thickness of $3.0\mu m$.

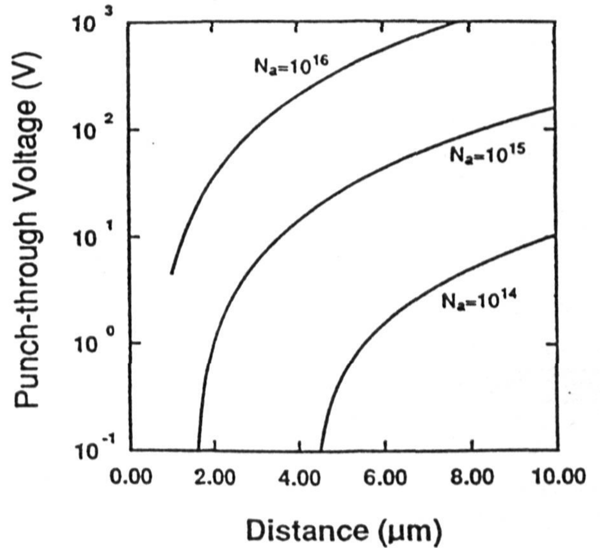

Figure 4: The dependence of the threshold voltage on the physical parameters. (Note: $N_t/N_a = 10$)