

(10-1)

## Modeling Deep-submicron MOS Devices for Circuit Simulation

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### Abstract

Important features of a deep-submicron MOSFET drain current model capable of supporting both digital and analog circuit simulations are described. Formulation of the commonly used mobility and velocity saturation models have to be revised to account for the influence of the higher electric field in deep-submicron devices. For analog circuit simulations, output resistance modeling and smooth transition from weak to strong inversion are important considerations. Some solutions are discussed.

### Introduction

MOS VLSI circuits have already entered the submicron era when the 90s' began. It appears certain that quarter-micron production MOS technology will be a reality within ten years. For device modeling engineers, the imperative job is to keep the device models in circuit simulators ahead of the advancing technology so that circuit designers can exploit the potential of a new technology as soon as it becomes available. Recently, we upgraded BSIM1 (Berkeley Short-channel IGFET Model, a digital-mainly micron-level model) to BSIM2 (a digital-analog capable deep-submicron model)[1][2]. This paper will describe the various issues we encountered in this endeavor. Emphasis will be placed on the drain current model.

Basic physics provides the guiding rules for device models. When developing device models for circuit simulation, however, issues such as computation efficiency and ease of convergence become very important. Some functional forms are preferred over others because they are more computationally efficient. Continuity of the charge, current, and their first and second derivatives with the terminal voltages in all regions is preferred because it often helps convergence.

### Modeling submicron MOSFET's

A one-micron CMOS technology typically has a gate oxide of about 20 nm, and junction depths of 0.3  $\mu\text{m}$  and 0.4  $\mu\text{m}$  for the n and p drain/source regions respectively. At the quarter-micron level, the gate oxide will be scaled down to about 75 Å, and the junctions will be shallower than 0.15  $\mu\text{m}$ [3]. Taking process variations into account, a device in this technology may have dimensions as small as 0.15  $\mu\text{m}$  and gate oxide as thin as 50 Å. Because of the extremely high oxide and channel electric fields that exist in this ultra-miniaturized device, many assumptions and approximations on which a micron-level model are based may not be appropriate anymore for a quarter-micron-level model especially if it has to be used for both digital and analog circuit simulations. In the following, we'll describe some of the necessary changes we found necessary.

#### *Mobility*

It is well known that the low-field surface mobilities of electron and holes follow universal expressions

having the general form[4] 
$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \left(\frac{E_{\text{eff}}}{E_0}\right)^n}$$
. In most device models, a linear approximation is used

in the denominator. For devices with oxide thinner than 100 Å, however, higher-order corrections are needed. Addition of a quadratic term was found to be adequate for oxide field up to 6 MV/cm as shown in figures 1 and 2. Since it was anticipated that the model will be used for both LDD and non-LDD devices,

no attempt has been made to include a separate expression involving the drain-source series resistance. It is lumped into the mobility parameters.

#### *Velocity saturation*

The shape of the I-V curve in both the triode region and the saturation region is affected by how the velocity saturation effect is modeled. Using a two-section model (model "2" in figure 3)[5] usually results in the second derivative of the drain current being discontinuous at the triode-to-saturation transition. After evaluating the benefits and drawbacks of various approaches, we've settled on a simple extension of the two-section model (model 3 in figure 3).

#### *Weak to strong-inversion transition*

Modeling the weak to strong-inversion transition is a difficult task. Piece-wise models are simple but are inaccurate around the transition region. They also produce discontinuities in the first derivative of the drain current at the transition. Surface potential based model such as the charge-sheet model[6], on the other hand, are too complex. So far, piece-wise models have done reasonably well for digital applications. As the gate oxide is thinned down and the power supply voltage is not scaled proportionally, however, the transition region becomes a significant portion of the power supply voltage, and achieving adequate accuracy is difficult even for digital applications. To alleviate this problem, we employed a cubic spline functional fit around the transition point. To guarantee that the transition is smooth for any oxide thickness, the transition points are determined in relation to the ratio of the gate capacitance and inversion-layer capacitance as shown in figure 4.

#### *Output resistance*

Analog circuit simulations require accurate modeling of the current and output resistance in the transition regions between weak and strong-inversion, and between triode and saturation[7]. Few existing models perform well in this regard. The physical phenomena responsible for the output resistance are well known. These include Drain Induced Barrier Lowering, Channel Length Modulation, and Hot Carrier Effect as shown in figure 5 [8]. Integrating them into one function which satisfies the continuity requirements turned out to be a demanding job. After weighing the available options, we decided to use a hyperbolic tangent based function for CML, and an exponential function for HICE as shown in figures 6 and 7. Note that both functions are not computationally efficient. We think a better solution may be using separate formulations for digital and analog applications.

### **Results and Discussion**

Some BSIM2 modeling results are shown in figures 8 to 10 for devices from our laboratories. In the past year, it has been also been tested on a wide range of CMOS technologies, including several sub-half-micron non-LDD and LDD technologies from several industrial laboratories, and was found to perform well. All tests were done using a simple custom parameter extractor. Extraction of a complete set of model parameters for a single device typically takes a few seconds excluding data taking time on an IBM PS/2 50 computer.

### **Conclusions**

If accuracy at high gate drive is all that is required, a micron-level MOSFET drain current model can be converted into a submicron capable model without much difficulty. Major changes are needed, however, if the model were to perform well at low current level and/or in analog circuit simulations. Inevitably, model complexity would increase with these changes and computational efficiency would suffer. It appears appropriate that an optimal model should include three levels with varied sophistication and capabilities. The most capable and thus the slowest level would be used for analog or analog/digital

circuit simulations, the middle level would be used for the simulation of critical digital signal paths, and the lowest level would be used for large digital system simulations.

### References:

- [1] M. C. Jeng, Ph.D. Thesis, 1990.
- [2] M.C. Jeng et al, p. 114, 1988 IEDM.
- [3] G. Baccarani, TED-31, p.452, April 1984
- [4] S.C. Sun and J.D. Plummer, TED-27, p.1497, Aug. 1980.
- [5] C. G. Sodini et al, TED-31, p. 1386, Oct. 1984.
- [6] J.R. Brews, SSE-21, p. 345, 1978.
- [7] Y. Tsvividis, p. 274, 1982 IEDM
- [8] P. Ko, p.489, 1985 IEDM.

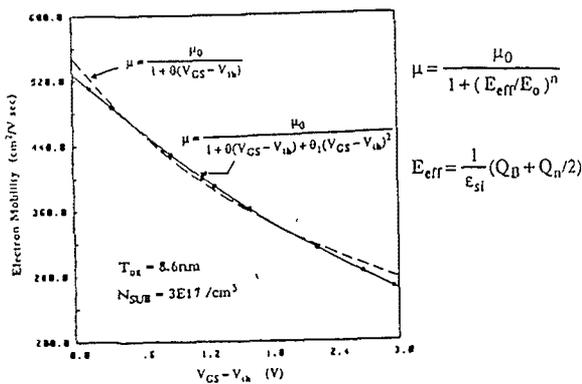


Figure 1. Various models for the electron surface mobility. The dashed line is the first-order model. The solid line is the second-order model.

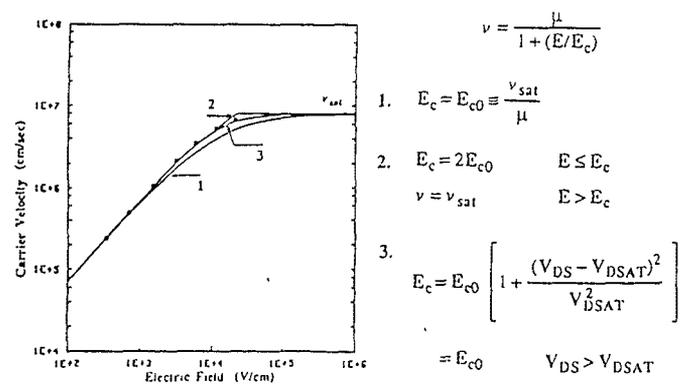


Figure 3. The electron velocity versus channel field.

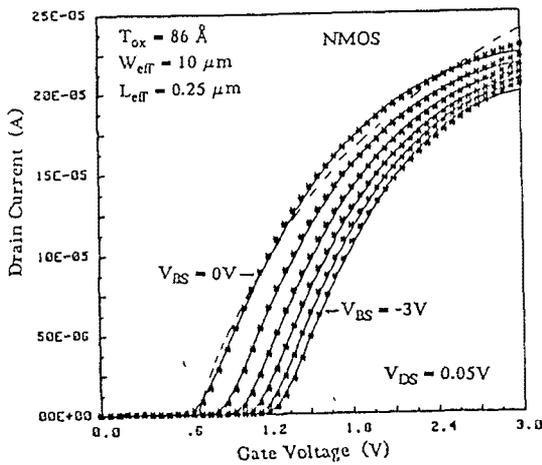


Figure 2. Measured and simulated  $I_{DS}$ - $V_{GS}$  in the triode region. Solid lines are the model and the asterisks are measured data. The dashed line is the best fit using the first-order model in figure 1.

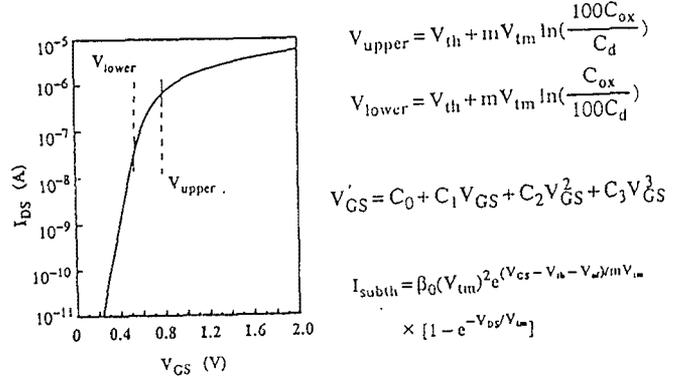


Figure 4. Modeling the weak to strong inversion transition.

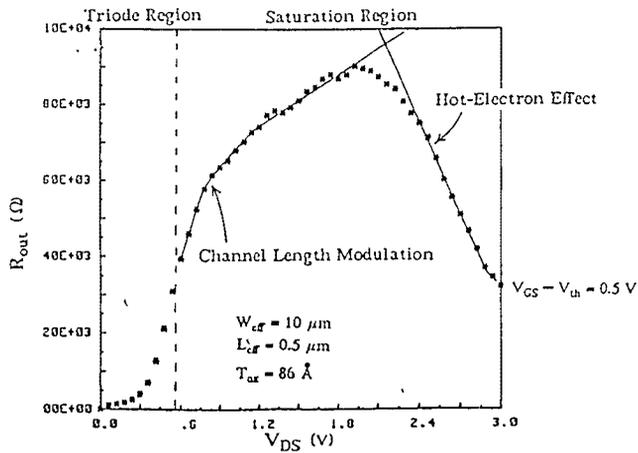


Figure 5. Factors affecting the output resistance.

$$I_{SUB} \propto I_{DSE} e^{\frac{-B_i}{V_{DS} - V_{DSAT}}}$$

$$I'_{DSAT} = I_{DSAT} (1 + C I_{SUB} R_{SUB})$$

$$= I_{DSAT} \left[ 1 + A_i e^{\frac{-B_i}{(V_{DS} - V_{DSAT})}} \right]$$

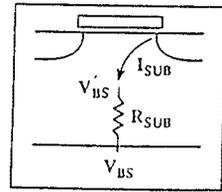


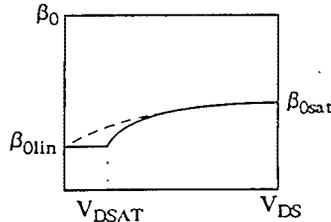
Figure 6. Modeling the Channel-Length Modulation

Physical Model:

$$\beta_0 = \beta_{0lin} \left( 1 + \frac{\Delta L}{L} \right)$$

$$\Delta L = \frac{1}{A} \ln \left[ \frac{A(V_{DS} - V_{DSAT}) + E_d}{E_{sat}} \right]$$

$$E_d = \sqrt{A^2 (V_{DS} - V_{DSAT})^2 + E_{sat}^2}$$



This Model:

$$\beta_0 = \beta_{0lin} + \beta_1 \tanh\left(\frac{\beta_2 V_{DS}}{V_{DSAT}}\right) + \beta_3 V_{DS}$$

Figure 7. Modeling the Hot-Carrier Effect.

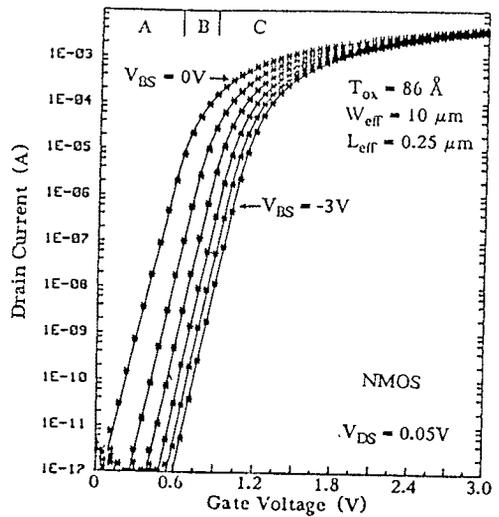


Figure 8. Modeled(solid line) and measured subthreshold characteristics of a 0.25 μm NMOSFET.

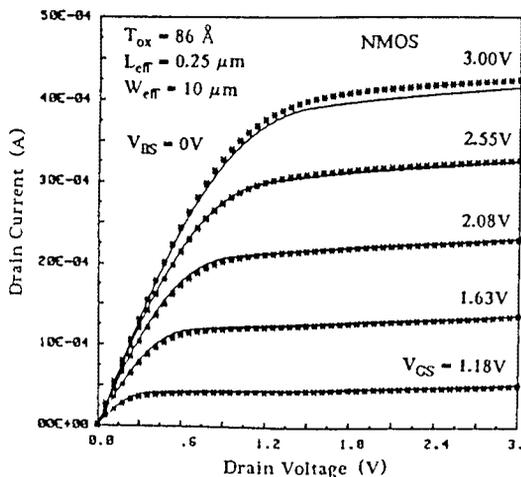


Figure 9. Modeled( solid line) and measured ID-VD characteristics of a 0.25 μm NMOSFET.

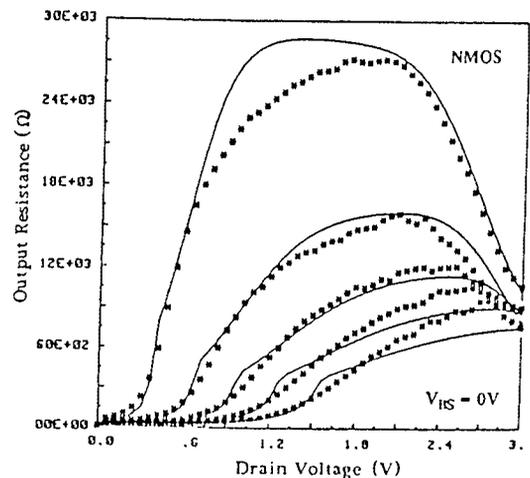


Figure 10. Modeled(solid line) and measured output resistance for the same device in figure 9