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SATURN - a Robust Process and Device Simulation System for Engineering Applications

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1 Introduction

The need for integrated process and device simulation tools has been recognized for several years now, e.g. [1, 2, 3]. In the first approaches efforts were focused on reducing the complexity of handling "stand-alone" simulation tools and providing interfaces between the simulation hierarchies. Applications were centered on predicting integral device quantities like $I(V)$ characteristics or leakage currents. However, as device dimensions enter the deep submicron regime the focus for device optimization shifts towards issues that are not easily accessible for routine simulations. For MOSFET optimization, as an example, three key issues may be identified:

i) the higher device complexity that has to be considered (e.g. the nonplanarity of the SiO_2/Si interface);

ii) physical effects that are no longer of second order importance (e.g. the point defect kinetics leading to laterally inhomogeneous channel doping [12]);

iii) optimization objectives that usually could not be considered at all due to a lack of appropriate physical modelling (e.g. the selfconsistent simulation of effects leading to device degradation [5]).

In consideration of these issues, our SATURN system aims at providing device engineers with a robust and proven "second generation" simulation environment, containing advanced simulators for the optimization of submicron devices. As the SATURN system is intended to be used as a "non-expert" tool to accompany the critical development phases of a technology, user friendliness and throughput are of prime importance. The user interface resides on a workstation while access to a remote high performance vector processor is fully integrated. An automatic book-keeping and file management system relieves the user of tedious control tasks.

2 The SATURN simulation system

In this section, the main components of the SATURN system will be briefly described (Fig. 1).

Process simulation

For the calculation of doping profiles, SIEMENS proprietary 1-D (POSEIDON) [7] and 2-D (MIMAS) process simulators are used. POSEIDON is compatible to SUPREM III on the input deck level but comprises advanced models for oxidation, diffusion (point defect kinetics [10]) and segregation [11] as well as improved algorithms (e.g. adaptive mesh). 1-D profile calculation is valuable for the optimization of MOSFET channel doping and for bipolar applications.

The MIMAS I program for planar structures is mainly used for the calculation of MOSFET source/drain structures. MIMAS I features a fully adaptive transient grid for implantation and diffusion. A vectorized version of the program reduces CPU time for the calculation of a complex

S/D structure to about 5 minutes. Accurate 2-D profiles have been shown to be essential for achieving predictive capability for reliability calculations.

MIMAS II is a general purpose process simulator for nonplanar structures. It includes patterning, implantation, oxidation (also oxide mechanics) and diffusion simulation. The oxidation and diffusion parts of MIMAS II use new numerical schemes which allow to simulate complex structures with reduced numerical effort [8, 9].

A "doping profile toolbox" program (PHOEBE) serves for combining several doping profiles into a complete device structure.

Device simulation

For the optimization of MOSFET devices a customized version of MINIMOS is implemented. In addition to the solution of the energy balance equation [4] we have enhanced MINIMOS by including the selfconsistent calculation of trap generation during a dc-stress experiment. This includes both the buildup of oxide charges and the generation of interface states. These enhancements enable us to look at the long term stability of the device under operating conditions using experimental data from short term dc-stress experiments [5]. Using doping profiles from MIMAS II, MINIMOS also simulates MOSFETs with nonplanar device geometries.

The program GALENE II [13] is included for general nonplanar device problems, e.g. storage trenches or isolation structures. MEDUSA/OSSI [14] with its possibilities for 1-D and quasi-2D/3-D simulations is taken for the optimization of bipolar transistors.

Circuit simulation

Parameters for compact circuit models are obtained from simulated $I(V)$ characteristics using the parameter extraction program JANUS which also serves for filling a table model data base. Both model options are available in our circuit simulator TITAN.

Supervisor program

The supervisor program serves as a common shell for all simulators and is embedded in a UNIX environment. While the specific input languages of the simulators (familiar to many device engineers) are not changed, the file handling and simulator call structure is standardized. Simple one-word commands are sufficient to invoke simulations.

A special feature of SATURN which is essential for user friendliness and acceptance by non-experts is the introduction of UNIX-type variables which can replace any keyword or value in the simulator input. The variables are exported to the overlaying supervisor shell. Thus, the necessary user control is reduced to just giving values for selected process steps while the supervisor program keeps track of the simulated variants in run-tables.

Making use of the integrated remote vector processing facility reduces the turn around time from a process change to new device and circuit parameters to a few hours.

3 Application examples

An example for the validity of the simulation results for submicron devices is given in Fig. 2 which shows the $I(V)$ characteristics for a MOSFET with a channel length of 60 nm. Excellent agreement between the SATURN simulations and experiment [6] is observed. Another example is given in Fig. 3 which shows a comparison of calculated and measured MOSFET lifetimes as a function of the reciprocal drain voltage for n-channel MOSFETs with different gate materials. Fig. 4 shows a MIMAS II simulation of the gate bird's beak formation at the drain edge of a MOSFET (poly-gate reoxidation). In Fig. 5 the MINIMOS results show the difference in simulated transconductance which can occur when the non-planarity of the gate edge is neglected.

References

[1] P. Lloyd, Proc. NASECODE III Conference, Galway (1983)

[2] K. Kato, N.Shigyo, T.Wada, S.Onga, M. Konaka and K. Taniguchi, IEEE ED-34, 2049 (1987)

[3] A.J. Strojwas and S.W. Director, Proc. Custom Integrated Circuits Conference (1987)

[4] W. Hänsch and S. Selberherr, IEEE ED-34, 1074 (1987)

[5] M. Orlowski, C. Mazuré, A. Lill, H.-M. Mühlhoff, W. Hänsch, A.v. Schwerin and F. Neppl, Proc. ESSDERC, Berlin (1989)

[6] G.A. Sai-Halasz, M.R. Wordeman, D.P. Kern, S. Rishton and E. Ganin, IEEE EDL-9, 464 (1988)

[7] H. Brand, G. Punz, W. Mader and H. Jacobs, to be published

[8] K. Steger and M. Paffrath, Proc. NUPAD III, Hawaii (1990)

[9] E. Rank and U. Weinert, Proceedings of this workshop

[10] M. Orlowski, Appl. Phys. Lett. 53, 1323 (1988)

[11] F. Lau, L. Mader, C. Mazuré, Ch. Werner and M. Orlowski, Appl. Phys. A 49, 671 (1989)

[12] M. Orlowski, C. Mazuré and F. Lau, Proc. IEDM, San Francisco (1987)

[13] W.L. Engl, R. Kircher, K.H. Bach and J. Götzlich, VLSI Process/Device Modeling Workshop, Tokyo (1987)

[14] W.L. Engl, R. Laur and H.K. Dirks, IEEE CAD-1, 85 (1982)

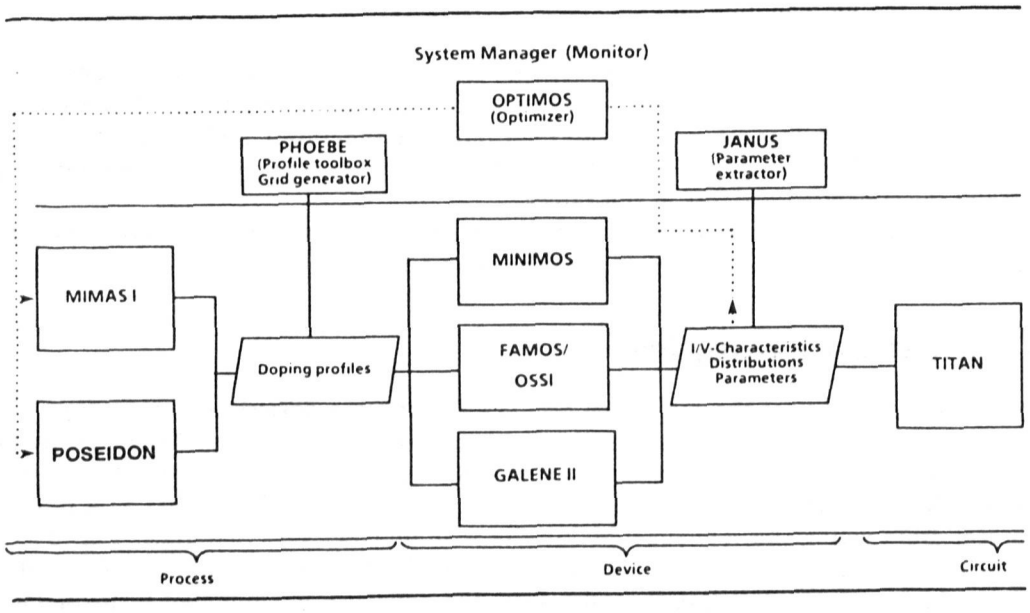

Fig. 1: Overview of SATURN system for the optimization of planar devices

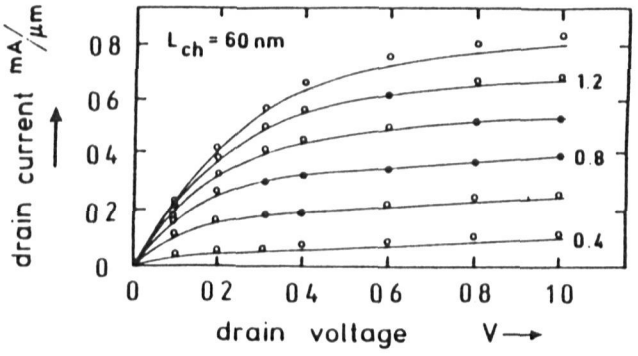

Fig. 2: Comparison of measured [6] and calculated output characteristics of N-channel MOSFET with a channel length of $60nm$ at 77 K. The standard mobility parameters in MINIMOS (also valid for 4M and 16M transistors) were used (full line: measurements, open circles: SATURN/MINIMOS).

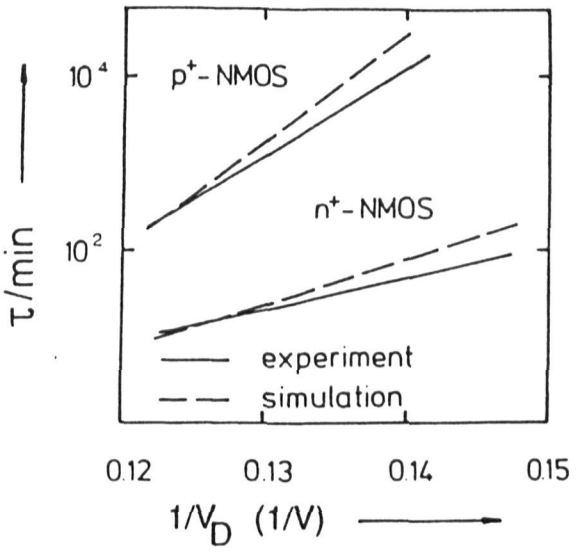

Fig. 3: Comparison of measured and calculated dependence of NMOS transistor lifetime on the reciprocal drain voltage for n^+ and p^+ polysilicon gates. Lifetime is defined as the stress time to a 2% change in drain current in the linear operating regime.

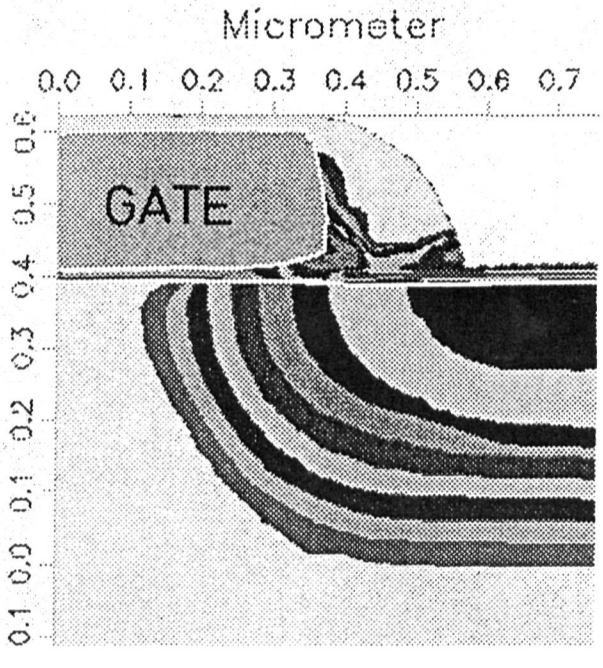

Fig. 4: MIMAS II simulation result: Device geometry and phosphorus doping contours for a MOSFET source/drain region. Process steps were i) LDD implantation, ii) first reoxidation, iii) etchback, iv) second reoxidation, v) spacer formation, vi) HDD implant, vii) drive-in. Note the gate bird's beak due to the polysilicon oxidation.

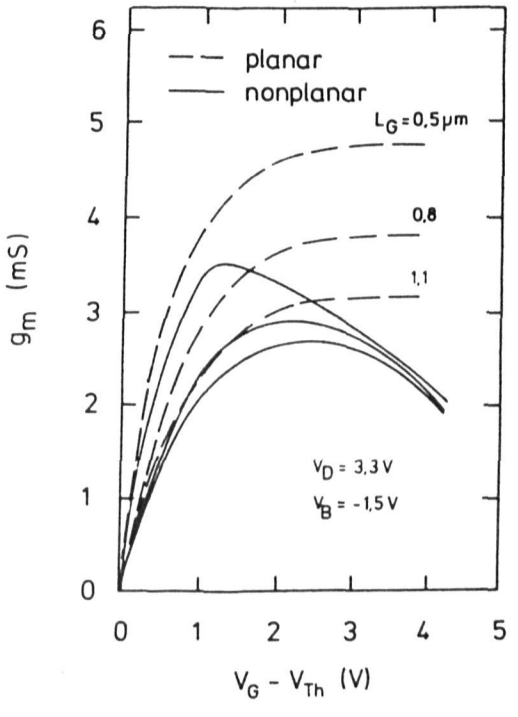

Fig. 5: Transconductance g_m of N-MOSFETs with different channel lengths ($W = 20\mu m, t_{ox} = 12nm$) as a function of the gate voltage above threshold (MINIMOS simulations). Depending on the geometry of the gate edge and the source/drain doping, the transconductance can be overestimated by a factor of two with planar simulations.