(5A-1)

DESIGN ASPECTS OF RESURF LDMOS TRANSISTORS

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The LDMOST is a common power device in HVIC's that is normally fabricated using the RESURF principle [1] (Fig. 1). The high voltage behaviour of such a device has been usually analyzed by means of numerical techniques. However, an analytical approach has been recently reported [2], providing more insight into the device physics. This paper is devoted to determine a suitable set of device properties (epilayer and substrate resistivities and epilayer thickness) for a given breakdown voltage requirement, while maintaining the constraint of a minimum ON-state resistance. The accuracy of our results has been confirmed by 2D simulations performed with CANDE [3].

From our analysis, based on the above mentioned formulation [2], sets of N_{sub}, N_{epi} and W_{epi} values can be obtained assuming the drift region length long enough to prevent premature avalanche breakdown at the superficial N^+-drain, and taking into account that the desired V_{BR} should be the one of the $N^+/N^-/P$ punch-through plane junction. In order to choice a suitable set of the above mentioned values, the ON-resistance has to be considered. The application in our case of a previous R_{ON} model [4], shows that R_{ON}*S has a minimum for a set of values with a very thin epilayer thickness, also confirmed by means of 2D simulations. Nevertheless, the breakdown voltage simulations show that the obtained V_{BR} is considerably lower than expected. The explanation of this behaviour arises from the analysis of the potential distribution inside the structure, which shows that the equipotential lines around the bulk metallurgical junction beneath the N^+-drain do not flatten, in contrast to the case of a thicker epilayer in which the equipotential lines flattening could be achieved (Figs. 2 and 3). Consequently, the reason why the obtained V_{BR} is lower than expected lies on the fact that the substrate-epilayer junction is no longer plane (mainly in the case of very thin epilayers), the equipotential lines around the bulk metallurgical junction coming from the superficial drain region vicinity.

Therefore, our criterion consists in forcing a voltage drop across the P-substrate at breakdown to be equal to the voltage at which the drift region is completely depleted; ensuring in this way that the equipotential lines around the bulk junction do not come from the drain proximity. Accordingly, only one set of the structure properties accomplishing this constraint is obtained (Figs. 4 and 5), and the breakdown voltages from the 2D simulations carried out are within 10% of the ideal bulk breakdown voltage, for different oxide thicknesses under the gate edge and for different ideal plane breakdown values (Fig. 6).

REFERENCES

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[2].- Z. Parpia and C.A.T. Salama. IEEE Trans. on Electron Dev., ED-37, 789 (1990).
[3].- J.A. Greenfield and R.W. Dutton. IEEE Trans. on Electron Dev., ED-27, 939 (1980). CANDE was obtained from Technology Modelling Associates, Palo Alto, CA, USA.
[4].- S. Colak. IEEE Trans. on Electron Dev., ED-28, 1455 (1981).

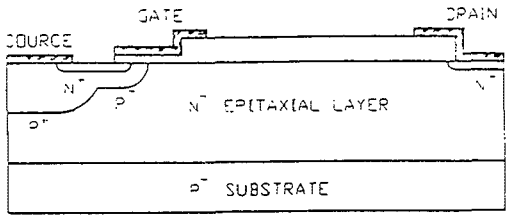

Fig.1.- Cross-section of the LDMOS transistor.

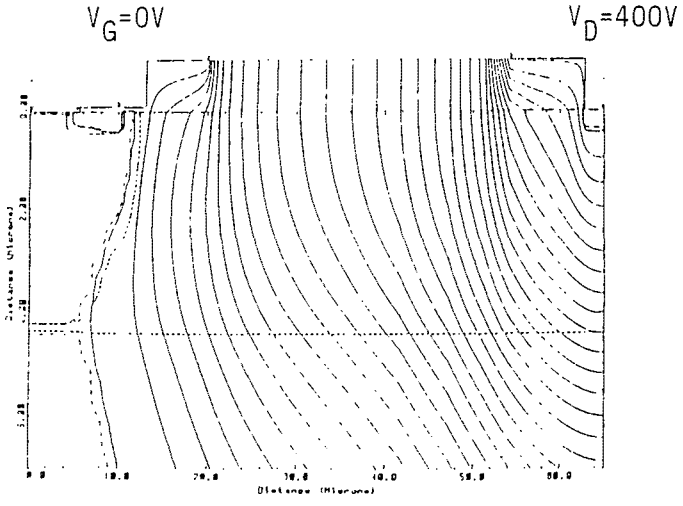

Fig.2.- Potential distribution in a RESURF LDMOST.
$N_{epi}=2.2x10^{15}cm^{-3}$, $N_{sub}=7.9x10^{14}cm^{-3}$
$W_{epi}=4.3um$, $L_{drift}=50um$, $t_{ox}=1um$.

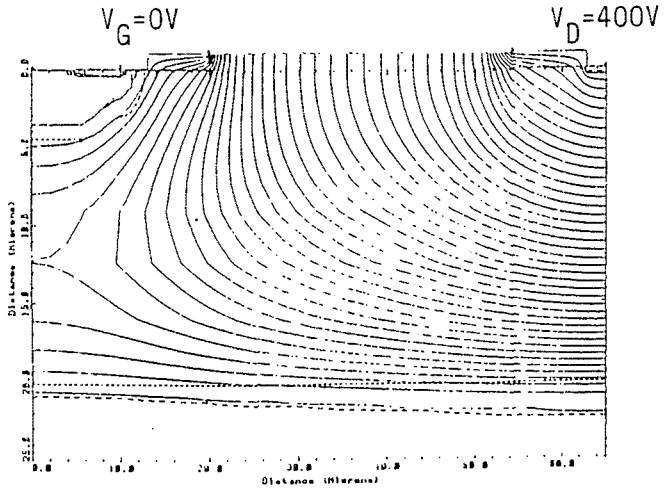

Fig.3.- Potential distribution in a RESURF LDMOST.
$N_{epi}=6.2x10^{14}cm^{-3}$, $N_{sub}=7.9x10^{15}cm^{-3}$
$W_{epi}=20um$, $L_{drift}=50um$, $t_{ox}=1um$.

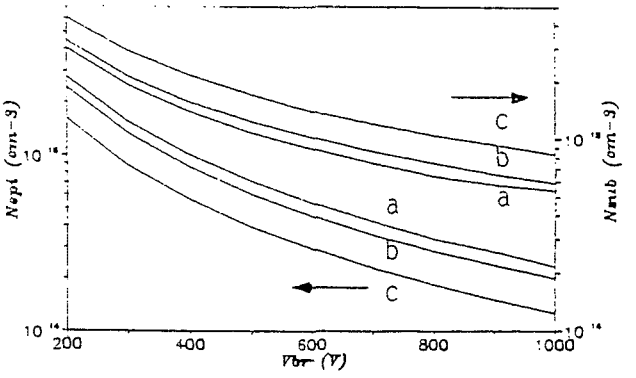

Fig.4.- Epilayer and substrate doping levels versus the expected breakdown voltage.
t_{ox}:a)1um,b)0.5um,c)0.1um.

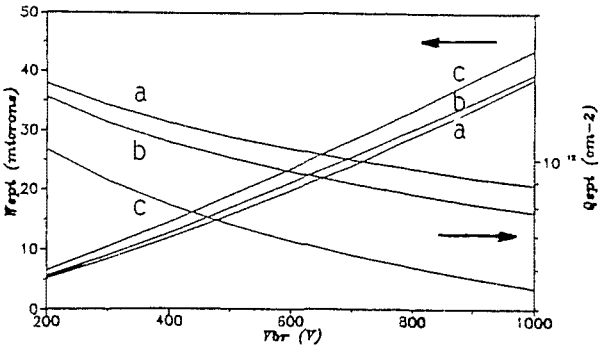

Fig.5.- Thickness and charge epilayer versus the expected breakdown voltage.
t_{ox}:a)1um,b)0.5um,c)0.1um.

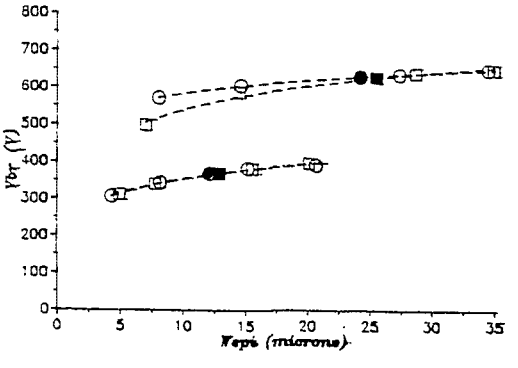

Fig.6.-Simulated V_{BR} for different set of device properties.
Expected values:400 and 700V.
t_{ox} : o 1um, □ 0.5um
solid points: devices according to the proposed model.