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Hot carrier analysis of MOSFET beyond the substrate current criterion

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Introduction: The substrate current as indicator for hot electron stability is well established/1/. However, especially, in the case of LDD devices it is known that this correlation is not always fullfiled. The injection process which is related to the field in the device is responcible for the accumulation of charge. Degrdation, however, is related to how these trapped charges influence the device's performance. We have developed a model that allows, fully self consistently, the calculation of spatial and temporal distribution of oxide and interface charge during a dc-stress experiment.

The model: The model consists of two steps/2/. In the first step we solve the full set of semiconductor equations for a given 2D device structure. This allows then to calculate the number of minority and majority carriers that can penetrate into the oxide region. In contrast to previous work we take heed of the fact that once the carriers are in the gate oxide they are no longer in a stationary state with the electric field wich changes abruptly at the interface. It requires the scattering by optical phonons to regain such a stationary state in the gate oxide. Therefore, as shown in Fig. 1, we have quasi ballistic carriers in the oxide (j_{noeq}), most prominently near the Si/SiO_2 interface, and those which are in a stationary state with the gate field (n_{ox}) and therefore obey a drift diffusion equation. For the latter ones we can solve their contunity equation with a source term that feeds the former to the latter by means of scattering. Having determined in this way the current distribution in the gate oxide region we can now solve a generalized trap equation in the 2D oxide region as the second step. This generalized trap equation describes the trapping scenario in a semi empirical way to allow the full competition of the most likely mechanisms such as shown in Fig. 2: electron trapping, hole trapping, interface state generation, and trap generation itself. An automatic time step control assures that the feedback of the oxide charges onto the silicon field is taken care of. This is especially important in PFET where accumulated negative charge has the tendency to reduce the electric field/3/. In Fig. 3 we show a distribution of negative oxide charge in a PFET for two different stress times. We see a more pronounced maximum of charge for larger stress time and a steepening of the charge profile on the drain side which comes from the negative voltage at the drain The spread of the charge distribution is approximately 100nm which is also found by different means/4/.

Substrate current criterion: We have used the trap model for an analysis of degradation data for different LDD NFET with oxide thickness 16nm. Doping profiles were obtained from 2D process simulation. We especially consider different LDD types for which the device lifetime results do not correlate with the expectations from the I_{sub} and I_{sub}/I_{DS} measurements. We specify the samples by A, B and C. Fig. 4a shows the effect of the LDD dose D_{LDD} and energy E_{LDD} on I_{sub}/I_{DS} as a function of the polySi gate length L_G. According to the results of Fig. 4a, we would expect the highest life time for case C and the lowest for case A. This is not confirmed by the degradation measurements, which are shown together with the calculated values in Fig. 4b. To analyze the degradation behaviour of the three samples, we calculated the time development of interface state generation during the stress experiment, in Fig. 5. For cases B and C, we find its maximum to be located outside the gate, and for A it is well below the gate. The surface doping at the location of the maximum interface states is largest for sample A ($5x10^{17}cm^{-3}$) and least for sample B ($1.4x10^{17}cm^{-3}$) and C ($3.1x10^{17}cm^{-3}$). Although A has the greatest number of interface states, their effect is screened by the high doping level Samples B and C require the same number of interface states for a 2% change in the drain current. The saturation (log-log scale!) indicated for A has its origin in the tendency of the acceptor-like interface states to turn themselves off. Moving the Fermi level toward the conduction band edge produces a higher negative interface charge, which in turn reduces the electron density and moves the Fermi level toward the middle of the bandgap.

Conclusions: We have developed a simulation tool that allows to directly monitor the spatial and temporal charge built up in the gate oxide region of a MOSFET device and its subsequential influence on the device performance. With this tool we can clearly demonstrate why the substrate current cretirion for hot carrier hardeness fails for LDD with weak overlap. It further more gives the device enegineer the new obtion to go beyond the substrate current creterion in the evaluation of a proper drain engineering for the best device.

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/2/Hänsch W; The drift diffusion approximation and its applications in MOSFET modeling. (Springer Wien New York to appear 1990/91) Chapt.V
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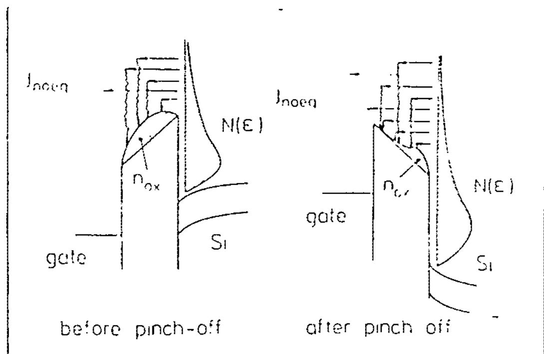


Fig. 1: Carrier injection into the gate oxide. The injected carriers j_{noeq} are in a non stationary state with the gate field. They relax due to collisions with phonons into a stationary distribution n_{ox} with the oxide field. After pinch-off there is a depth dependent threshold.

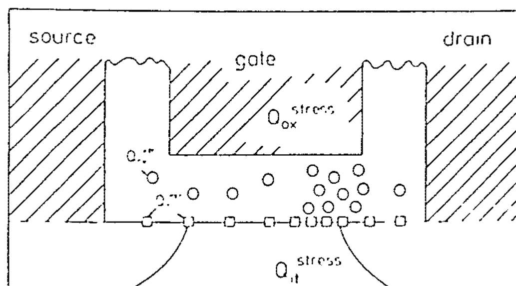


Fig. 2: Distribution of traps in the gate oxide. Open circles - oxide traps; open squares - interface states. There is a process dependent intrinsic background of oxide traps and interface states prior to the stress induced damage.

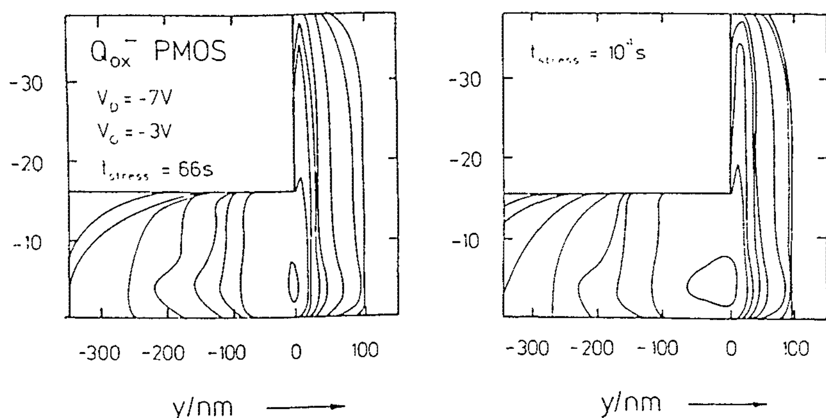
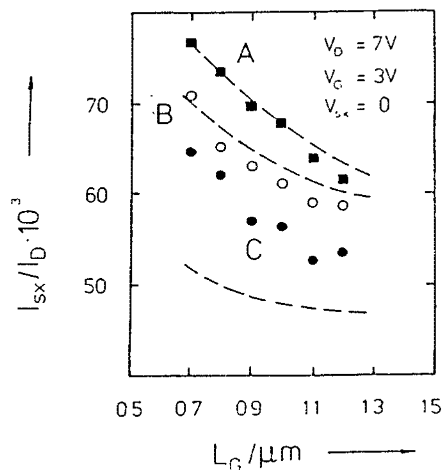


Fig. 3: Distribution of negative oxide charge for stress time t=66s (left) and t=10^4s (right). The origin y=0 corresponds to the drain side gate edge. The oxide thickness is 10nm.



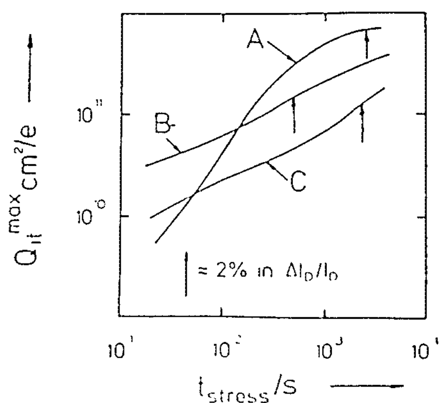


Fig. 5: Time evolution of the maximum interface state charge during the stress experiment for the LDD type devices A, B and C as defined in Fig. 72. The arrows refer to the time when 2% change in drain current in the linear mode was reached.

Fig. 4: (a)Substrate current versus drain current for different LDD type devices at different gate length L_G.(b) Life time of different LDD type devices for LG=1μm. The life time was determined by a 2% change of the drain current in the linear mode. open circles - A: LDD with 4·1013cm-²/60keV, filled squares - B : LDD with 3·1013cm²/60keV, filled circles - C: LDD with 3·1013cm-²/80keV Symbols - experiment; dashed lines - simulation