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Two-Dimensional Transient Analysis of a BiNMOS Transistor Operating at 77K using a modified PISCES Program

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Abstract

This paper presents a detailed two-dimensional numerical simulation study on the steady state and the turn-on transient behavior of a BiNMOS device operating at 77K using PISCES with modified low-temperature models. The 2D lateral base effects on the steady state performance of the bipolar transistor at $77K$ are different from that at $300K$. The turn-on transient performance of the BiNMOS device shows that, at $77K$, the switching time, which is determined by the load-related delay and the intrinsic delay of the bipolar device, increases about 39% from its $300K$ value for an output load of $0.1pF$.

Summary

Recently, BiCMOS technology has been emerging as one of the major technology for high speed VLSI circuits. During the pull-down transient of a BiCMOS inverter, NMOS and the bipolar devices are the most important part. For low-temperature operations, the performance of BiCMOS circuits can be quite different. In this paper, the low-temperature steady state and transient behavior of a BiNMOS device is studied based on a 2D device simulator–PISCES-2B [1] with modified low-temperature models.

Fig. 1(a) shows the cross section of the BiNMOS device. An NMOS device without an LDD structure has been used in the study. The NMOS device has an effective channel length of $0.9\mu m$, a gate oxide thickness of $250\AA$, and a threshold voltage of $0.8V$. The NMOS device and the bipolar device are placed against each other separated by an oxide of $5000\AA$. The base and the source terminals are wired together with a parasitic capacitance of $0.1fF$. The collector and the drain contacts are connected by an interconnect where an output capacitive load of $0.1pF$ is placed. Fig. 1(b) shows the vertical doping profile in the intrinsic and the extrinsic base regions. The intrinsic base has a width of $0.1\mu m$ and a peak concentration of $1 \times 10^{18} cm^{-3}$. For simplicity, metal contact to the emitter has been used. Gaussian vertical profiles and lateral straggles equivalent to 80% of the vertical ones have been assumed in the intrinsic and extrinsic base regions. A 2D device simulator, PISCES-2B with modified low-temperature models has been used to evaluate the performance of the BiNMOS transistor at $77K$. The modified models used in the low-temperature BiNMOS transistor analysis include incomplete ionization, concentration and E-field dependent mobilities, Shockley-Read-Hall and Auger recombinations with concentration dependent lifetimes [2]. To overcome convergence problems for low-temperature simulation, Newton's method with Gaussian elimination of the Jacobian for two-carrier simulations with appropriate scaling is used.

Fig. 2 shows the steady state performance of the NMOS device used in the BINMOS transistor. Fig. 2(a) shows the I_D vs. V_{GS} curves for $V_{DS} = 0.1V$ and $3V$. Solid lines show the results for the $77K$ case and the dashed ones for the $300K$ one. The subthreshold slope improves about 3.8 times for the $77K$ case. Due to the $0.9\mu m$ channel length, the drain induced barrier lowering effects are slightly less for the $77K$ case [3]. In the strong inversion, the $77K$ case shows larger drain currents. Fig. 2(b) shows the the I_D vs. V_{DS} curves for V_{GS} from $1V$ to $5V$. In the saturation region, the drain currents for the $77K$ case improve about 50%. Fig. 3 shows the steady state performance of the bipolar device used in the BiNMOS transistor, biased at a V_{CE} of $3V$. Fig. 3(a) shows the current gain of the bipolar device at $300K$ and $77K$. The $77K$ case shows a greater than $10\times$ disadvantage in current gain. At a high current level, the gain falls off owing to the 2D base push-out effects for both cases. At a low current level, the current gain falls off at a higher current level for the $300K$ case due to a much larger base generation effect in the space charge region. Fig. 3(b) shows the base resistance, which is extracted by measuring the voltage drop between the base electrode and the center of the intrinsic device area. At a current level below $10^{-5} A/\mu m$, the $77K$ curve shows a larger base resistance due to carrier freezeout effects. At a high current level above $10^{-5} A/\mu m$, the $300K$ case shows a higher base resistance due to a higher mobility at $77K$. The unity gain frequency, f_T, is calculated according to Gummel's formula. Fig. 3(c) shows the f_T vs. I_C curves at $77K$ and $300K$. The $77K$ case shows a lower peak in f_T due to the presence of compensating donor levels at $77K$ [4]. Fig. 3(d) shows the base-to-emitter capacitance vs. I_C curves at $77K$ and $300K$. The zero-bias base-to-emitter capacitance for the $77K$ case shows a lower value of $2fF$, compared to $3fF$ at $300K$ due to freeze-out effects. On the other hand, the diffusion capacitance of $77K$ case is much higher at a high current level owing to a lower thermal voltage [4]. Fig. 4 (a) and (b) show the 2D electron concentration contours at collector currents of $10^{-7} A/\mu m$ and $10^{-4} A/\mu m$ respectively. At a collector current of $10^{-7} A/\mu m$, the $77K$ case shows a much larger base-collector space charge area, which is correlated to a larger base resistance and a smaller base-to-emitter capacitance. On the other hand, at a collector current of $10^{-4} A/\mu m$, the $300K$ case has a more base pushout behavior in the intrinsic device area. However, at $77K$, in the extrinsic base region, more electrons exist, which is correlated to a lower base resistance and a higher base-to-emitter capacitance.

For a BiNMOS transistor, steady state parameters cannot accurately describe the behavior of the device during the transient operations. In order to study the overall performance of the BiNMOS transistor at $77K$, turn-on transient analysis is now described. By imposing a voltage step from $0V$ to $5V$ in $10ps$ at the input, the turn-on transient behavior of the BiNMOS device has been obtained for both the $300K$ and $77K$ cases. Fig. 5(a) and (b) show the base voltages and currents for both the $300K$ and $77K$ cases during the first $50ps$ period. There are overshoots in the base voltage and current for both cases around the edge of the input ramp. The peak in V_B is determined by the gate-to-source overlapped capacitance and the total equivalent capacitance at the base node - mainly the parasitic capacitance (C_P) and the base-to-emitter capacitance (C_{BE}). The $77K$ case shows higher overshoots in both the base voltage and current. Fig. 6 shows the output voltages for two cases during the overall $1ns$ period. Also shown in the figure are the output voltages during the turn-on transient at $300K$ and $77K$ of an NMOS device without the bipolar transistor. For the BiNMOS device, the switching time, defined as the time from the middle of the input swing to the middle of the output swing, degrades from $0.31ns$ at $300K$ to $0.42ns$ at $77K$. This can be attributed to a smaller bipolar current drive and a larger base diffusion capacitance despite a smaller base resistance and a higher NMOS current drive at $77K$. On the other hand, the switching time of the NMOS device improves from $0.75ns$ at $300K$ to $0.47ns$ at $77K$ owing to the mobility enhancement at 77K. Fig. 7(a), (b) and (c) show the base voltage, the base and the collector currents during the transient. After the input ramp-up period, the base voltage decreases slowly. In the mean time, the base current maintains steady and the collector current is increasing monotonically. The base voltage for the $77K$ case is much larger than the $300K$ one during transient. At $0.3ns$, the collector current reaches a higher peak for the $300K$ case. As for the $77K$ case, the collector current reaches its peak around $0.45ns$. After peaks in collector currents, both the base and the collector currents are decreasing, which indicates the carriers in the base are being removed.

The BiNMOS has a unique charge buildup and collapse process in the bipolar device region during the turn-on transient at $77K$. The switching speed of the BiNMOS transistor at $77K$ is dominated by the load related extrinsic delay and the internal intrinsic delay of the bipolar device. The load related extrinsic delay is determined by the load capacitance and the current drive of the BiNMOS device during transient. As for the intrinsic delay of the bipolar device, it's mainly determined by the product of the base resistance and the base-to-emitter capacitance and the total amount of electrons to build and to remove during transient. In spite of a larger current drive during transient at $300K$, the electrons in the bipolar device needed to build and to remove at $300K$ are also much more. As a result, the intrinsic delay of the $300K$ case is not proportionally smaller compared to the extrinsic delay.

More insight into designing bipolar devices for BiNMOS circuits can be obtained by examining the 2D carrier distrubitions in the bipolar device at peaks of their collector currents during transient. Fig. 8(a) and (b) show the 2D hole(p) and electron(n) concentration contours for the $300K$ case at $0.3ns$ and the $77K$ case at $0.45ns$. From the 2D hole concentration contours, a much less high injection phenomenon is observed at $77K$. From the 2D electron concentration contours, the $77K$ case shows a less severe base push-out behavior in the intrinic device area. On the other hand, more electrons exist in the extrinsic base area at $77K$. However, total electrons in the overall base area are still much less at $77K$. Therefore, the extrinsic base of the bipolar device in the BiNMOS transistor influences not only the extrinsic delay but also the intrinsic delay dominated by the electron transfer process and the product of C_{BE} and the base resistance. Consequently, for a large load at the output, steady state performance of the bipolar device should be emphasize to reduce the extrinsic delay for $77K$ operation. For a small output load, the intrinsic delay resulting from the bipolar internal charge build-up and removal should be focused.

Acknowledgments

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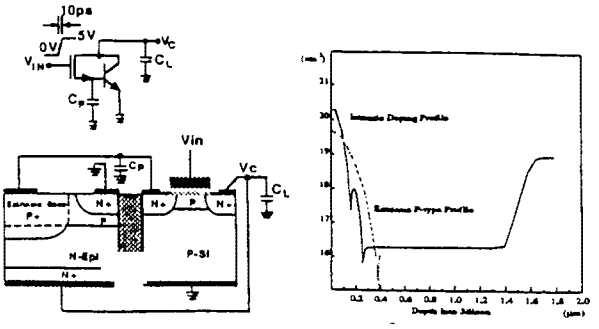

Fig 1 (a) The BiNMOS device structure under study. (b) Vertical doping profiles in the intrinsic and the extrinsic base areas.

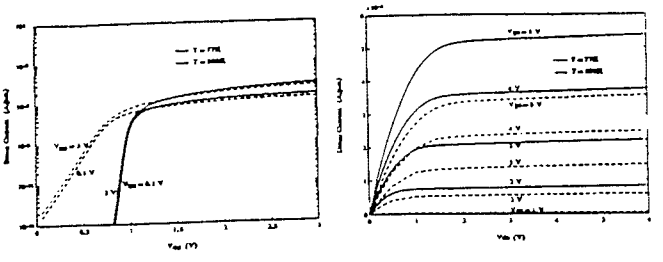

Fig. 2 (a) The I_D vs. V_{GS} curves of the NMOS device, used in the BiNMOS transistor, biased at V_{DS} of $0.1V$ and $3V$ for the $77K$ and $300K$ operations. (b) The I_D vs. V_{DS} curves of the NMOS device biased at V_{GS} from $1V$ to $5V$ for the $77K$ and $300K$ operations.

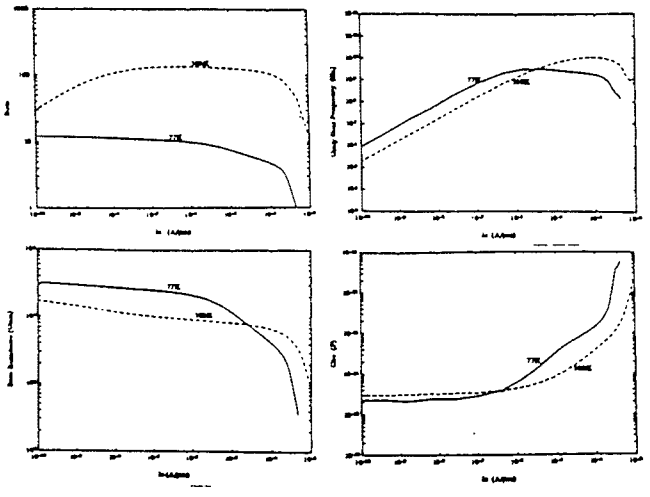

Fig. 3 Small signal steady state performance of the bipolar device used in the BiNMOS transistor, biased at a V_{CB} of $3V$ for the $77K$ and $300K$ operations. (a) The current gain. (b) The base resistance. (c) The unity gain frequency. (d)The equivalent base-to-emitter capacitance.

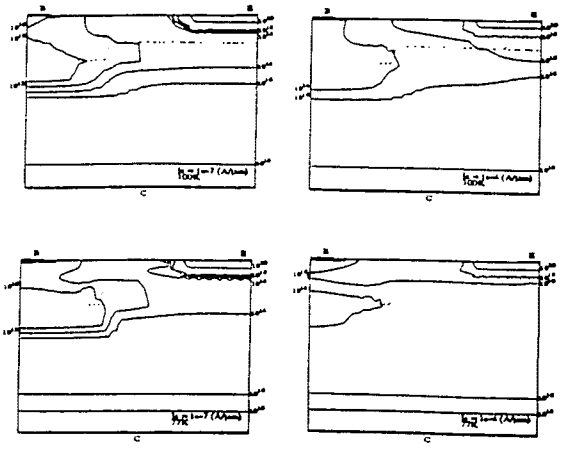

Fig. 4 The 2D electron concentration contours for the bipolar device biased at V_{CB} of $3V$ (a) At a collector current of $10^{-7} Amp/\mu m$. (b) At a collector current of $10^{-4} Amp/\mu m$.

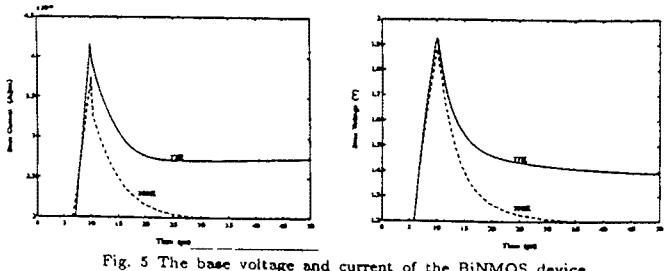

Fig. 5 The base voltage and current of the BiNMOS device during the initial $50ps$ period for both the $300K$ and $77K$ operations. (a)Base voltage. (b)Base current.

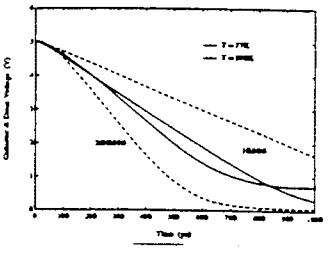

Fig. 6 The ouput voltage of the BiNMOS device and the NMOS device for both the $300K$ and $77K$ operations during the overall $1ns$ transient period.

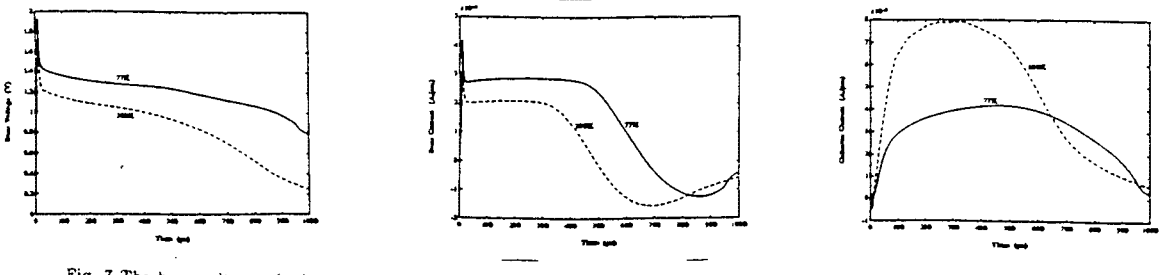

Fig. 7 The base voltage, the base current, and the collector current of the BiNMOS device during the overall $1ns$ period for both the $300K$ and $77K$ operations. (a)The base voltage. (b)The base current. (c)The collector current.

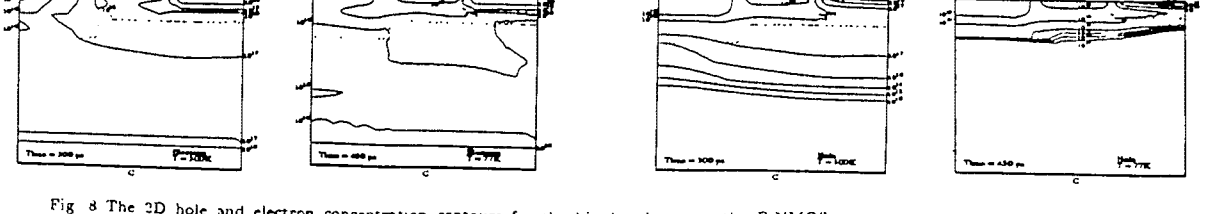

Fig 8 The 2D hole and electron concentration contours for the bipolar device in the BiNMOS transistor at $0.3ns$ for the $300K$ case and at $0.45ns$ for the $77K$ case. The metallurgical junctions are marked by the lightest lines. (a) Hole concentration contours (b)Electron concentration contours