Two Dimensional Device Simulator VENUS-2D/B for Amorphous Silicon using the Gap States Model

K.Sumino and T.Ishizuka
FUYO Data Processing & Systems Development, Ltd., Tokyo,Japan
M.Hirose
Research Center for Integrated Systems, Hiroshima Univ., Higashi-Hiroshima, Japan

INTRODUCTION

Two dimensional device simulator for crystal silicon is widely used[1], and we have developed the two dimensional two carrier device simulator VENUS-2D/B.[2] Also, we have newly added capability of analyzing an amorphous silicon device to VENUS-2D/B. In this paper,the characteristics of an inverted-gate amorphous silicon thin film transistor (TFT) are simulated by VENUS-2D/B.

NUMERICAL DEVICE MODELING

The basic equations for amorphous semiconductor devices can be described as follows:

$$\nabla(\varepsilon \nabla \Psi) = q(N_D - n_C - n_T) . \quad (1)$$

$$\nabla(J_n) = 0 . \quad (2)$$

Here, $J_n = -q(\mu_n n_C \nabla \Psi - D_n \nabla n_C)$ and $D_n = (kT/q)\mu_n$.
These two equations are solved for the potential Ψ and the free electron density n_C, and the trapped electron density n_T is calculated by using the values of Ψ and n_C.
Using Gummel's iterative scheme, the nonlinear system is linearized. Linearized Poisson's equation is expressed as follows:

$$\nabla(\lambda \nabla \Psi^{K+1}) - (n_C^K + (\partial n_T/\partial \Psi)^K)(\Psi^{K+1} - \Psi^K) - n_C^K - n_T^K + N_D = 0 . \quad (3)$$

MODELING OF TRAPPED ELECTRON DENSITY

Considering the gap state distribution N(E) in amorphous silicon, the trapped electron density n_T is given by

$$n_T = \int_{E_C-(E_C^0-E_F^0)}^{E_F} N(E)\,dE , \quad (4)$$

where, E_F is the quasi-Fermi level for electron, E_C the conduction band energy, E_C^0 the conduction band energy at the thermal equilibrium, and E_F^0

the equilibrium Fermi level.

The gap state density distribution for hydrogenated amorphous silicon can be given by the combination of exponential functions.[3]

$$N(E)=10^{15}[A+B\{\exp(\frac{E-E_C+0.6}{0.05})+\exp(-\frac{E-E_C+1.0}{0.05})\}$$
$$+C\{\exp(\frac{E-E_C+0.5}{0.025})+\exp(-\frac{E-E_C+1.1}{0.025})\}] \quad (cm^{-3}eV^{-1}), \quad (5)$$

where A,B,C are parameters.

RESULTS AND DISCUSSION

An inverted-gate TFT structure and an example of the analyzed characteristics are shown in Figs.1 and 2, respectively. By taking into account the trapped electron density in the amorphous silicon gap states, the TFT characteristics can be obtained and the validity of the two dimensional device simulator VENUS-2D/B is demonstrated.

ACKNOWLEDGMENTS

The authors would like to especially thank Prof.M.Koyanagi, Reserch Center for Integrated Systems, Hiroshima University for valuable discussion.

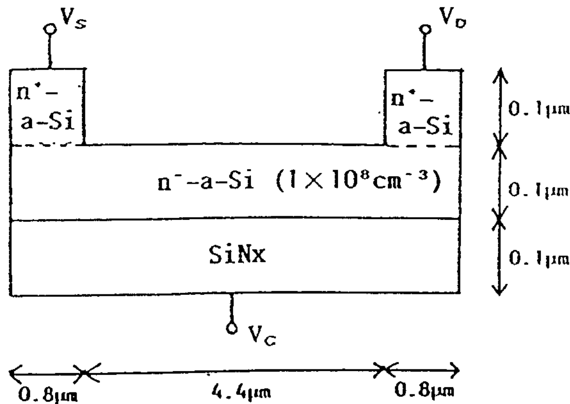

Fig.1. Cross Sectional View of an inverted-gate TFT

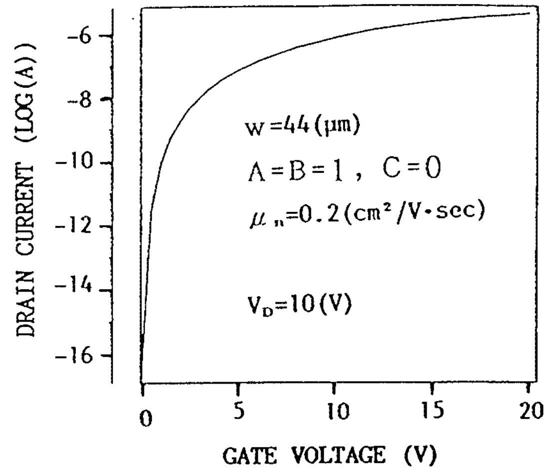

Fig.2. I_d-V_g characteristic for an inverted-gate TFT shown in Fig.1.

REFERENCES

1) T.Toyabe et al. : Proc. NASECODE I (Bool Press) (1979), P.290.

2) Y.Iriye and T.Ishizuka: Proc. of 1988 IEEE SOS/SOI TECHNOLOGY WORKSHOP (1988), P.43.

3) T.Suzuki,Y.Osaka,and M.Hirose: Jpn. J. Appl. Phys. 21 (1982) L315.