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# A MODEL FOR THE ELECTRIC FIELDS IN GATE-OFFSET STRUCTURED LDD MOSFET's

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The lightly doped drain(LDD) structures have received a considerable attentions due to a successful reduction of the lateral electric field in the short channel MOSFET's. It is well known that the maximum electric field(Emax) critically controls the hot carrier induced degradation in submicron MOSFET's so that the channel electric fields in LDD MOSFET's have been rigorously characterized both numerically and analytically. Numerical analysis by 2-D simulators may provide a fairly accurate result. However, device physics dictating various phenomena may not be easily interpreted by numerical analysis besides 2-D simulations are time consuming and costly so that an accurate analytical model may be desired.

Semi-quantitative analytical models for short-channel LDD MOSFET's have been developed by several groups (1,2,3). Although, the channel electric field have been modeled quite well, most of previous models may be applied to the limited LDD structures. A model for the LDD structure with a full overlap rather than a realistic gate-offset one have been reported.(1) Recently, models for the gate-offset structures have been developed.(2,3) However, those models have assumed a uniform lateral doping profile rather than a Gaussian one so that the lateral diffusion of dopants in the lightly doped drain region is neglected. Furthermore, the junction depth of the lightly doped region is assumed to be identical to that of heavily doped drain while a junction depth of the lightly doped drain in real devices is much shallower than that of the heavily doped

THe purpose of this work is to present an analytical model for the gate-offset structured LDD MOSFET where the doping profile of the lightly doped region is a Gaussian rather than widely used uniform one. Our model also choose an arbitrary junction depth ratios of the lightly doped drain to the heavily doped drain. The LDD structure considered in our work is shown in Fig. 1. The lateral electric field distribution is successfully obtained by solving Gauss's law with proper boundary conditions in the velocity saturated region as indicated in Figure 1. The fringing electric field effects is neglected because the maximum electric field in the channel may not be influenced much by the fringing fields. The lateral field gradient near pinch-off point has been also neglected.

The validity of the model is verified by comparing our results with 2-D device simulators such as MINIMOS. As seen in Figure 2 and 3, it is found that the results of our model agree well with those of numerical simulations. From our model, We are able to predict effects of various device geometry and bias conditions on the channel field distributions.

(1) K. Terrill, C. Hu, and P. Ko, IEEE Elec. Dev. Lett. p440, Nov. 1984
(2) K. Mayaram, J. Lee and C. Hu, IEEE Tran. Elec. Dev. p1509, July, 1987
(3) J. S. T. Huang, IEEE Tran. Elec. Dev. p1158, July, 1988

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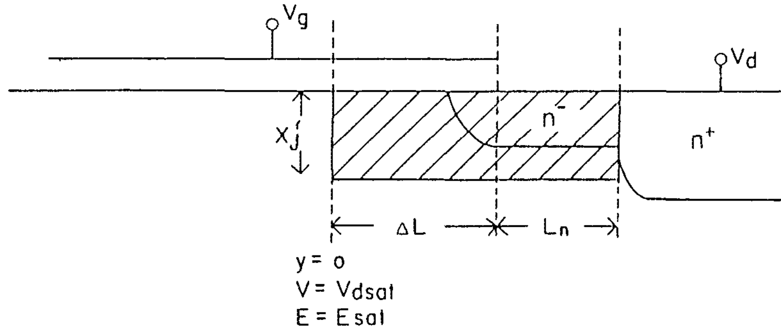


Fig.1 Cross section of LDD device structure of our model.

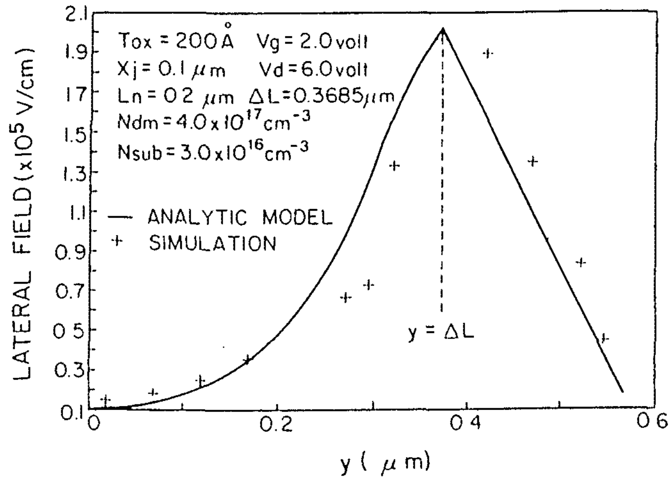


Fig.2 Lateral electric field versus distance. ( oxide thickness : 200 A, LDD junction depth : 0.1 μm, $n^+$ drain junction depth : 0.2 μm, peak concentration of the lightly doped region assumed Gaussian : 4.0 × $10^{17} cm^{-3}$ )

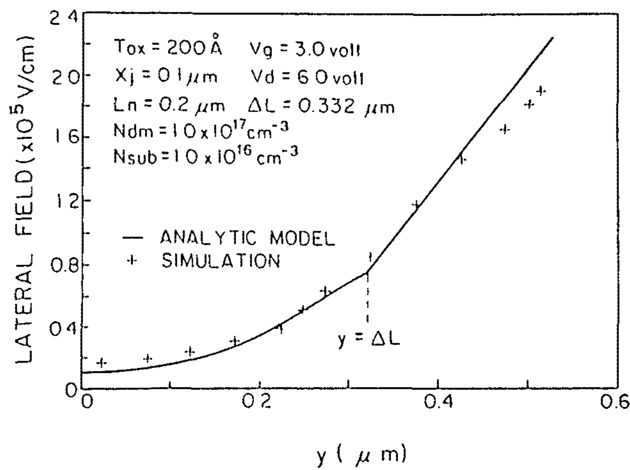


Fig.3 Lateral electric field versus distance. ( oxide thickness : 200 A, LDD junction depth : 0.1 μm, $n^+$ drain junction depth : 0.2 μm, peak concentration of the lightly doped region assumed Gaussian : 1.0 × $10^{17} cm^{-3}$ )