# Characterization of Shallow Trench-Isolated n-MOSFET with Sidewall Implantation using a 3-D Device Simulation

K. Ohe and S. Odanaka

Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd.
Moriguchi, Osaka 570, Japan

## Introduction

It is well known that MOSFETs with a shallow trench isolation (fully recessed isolation oxide) show an inverse-narrow-width effect. This effect has been explained by the contribution of the channel edge current induced by fringing electric field [ 1 ]. To suppress this undesirable structural effect, the use of large tilt-angles during implantation into the sidewalls [2] has been proposed. The development of the trench-isolated MOSFET with sidewall boron profile becomes important to realize high packing density CMOS VLSIs.

In this report, the "narrow-width effect" of this n-MOSFET is characterized by using experimental data and numerical results from a 3-D process/device integrated simulator - SMART [3].

## Narrow-Width Effect and Edge Current of Trench-Isolated MOSFET

The trench-isolated MOSFETs were fabricated down to channel widths of 0.5μm using a novel planarization process with an etch-stop (PRORPS) [4], and sidewall implantation technology. Fig. 1 shows a simulated impurity profile and isolation oxide shape according to the PRORPS process. At the top corner of the silicon the higher boron concentration is formed by sidewall implantation. Fig. 2 compares the experimental data and simulated results of threshold voltage versus channel width. The device shows the "narrow-width effect" with the excess boron doses implanted in the sidewalls. To understand the "narrow-width effect", we can see in Fig. 3 the simulated electron current densities at the surface. The edge current is enhanced with the reduction of the channel width although the corresponding results in Fig. 2 show the "narrow-width effect". This is because the boron implanted in sidewalls extends toward the channel center as the channel width is reduced and its concentration is increased [5]. The 3-D simulation reveals that the devices show the "narrow-width effect" although the edge current is enhanced.

The channel edge current is affected by the shape of the top corner of the trench isolation. Fig. 4 (a)-(b) shows the 3-D simulation results assuming two kinds of corner shapes. The experimental data also shows $I_D$-$V_G$ characteristics of 1.36-, and 0.46-μm channel width devices with a sidewall implantation which show the "narrow-width effect" in Fig. 2. For the W=1.36μm device, Fig. 4 (a) indicates that the trench corner shape has little impact on the drain current when a backgate bias is applied. In this case, the edge current is suppressed as shown in Fig. 3. While for the W=0.46μm device having the edge current, as shown in Fig. 4 (b), the subthreshold current is strongly enhanced by the backgate bias because of the fringing field effect. The devices which exhibit the edge current are very sensitive to the top corner shape of the trench isolation. In trench-isolated MOSFETs with sidewall implantation as well as conventional trench isolated MOSFETs, it is necessary to suppress this edge current.

## Conclusion

We have characterized the threshold behavior of the trench-isolated n- MOSFETs with sidewall implantation using the experimental data and the 3-D process/device integrated simulations. It is found that the lateral diffusion of the boron implanted in the sidewalls induces an enhancement of the edge current although the devices show the "narrow-width effect". The devices which exhibit the edge current are very sensitive to the top corner shape of the trench isolation

## References


[1] N. Shigyo et al., Symp. on VLSI Tech. Sept. 1982, pp. 54 - 55.

[2] G. Fuse et al., IEEE Trans. Electron Devices, vol. ED - 34, pp. 356 - 360, Feb., 1987.

[3] S. Odanaka et al., in 1987 ISCAS Proc., vol. -2, pp. 534 - 537, 1987.

[4] G.Fuse et al.,in IEDM,Dig. Tech. pp.732 - 735, 1987.

[5] S. Ohe et al., IEEE Trans. Electron Devices to be published.


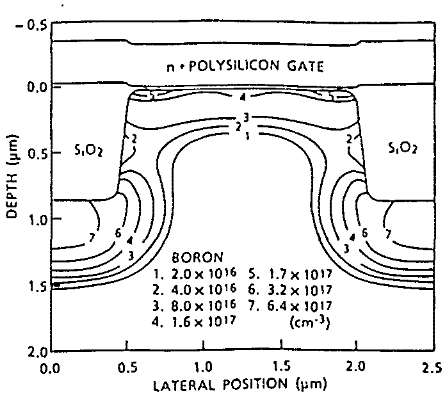


Fig.1 The simulated impurity profile of the n-MOSFET with the sidewall implantation. The channel width is 1.36μm.

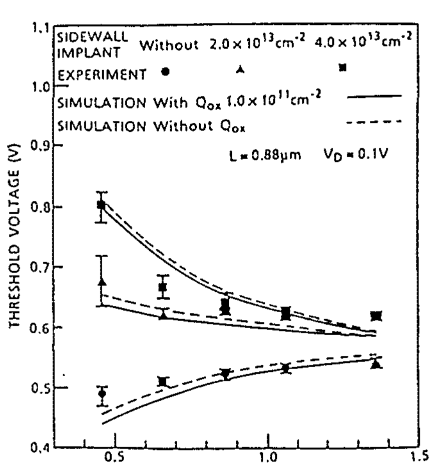


Fig.2 Comparison between the experimental data and simulations of the Vth - W.

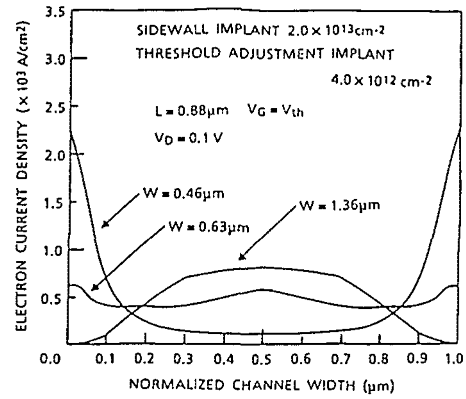


Fig.3 The electron current densities at the surface.

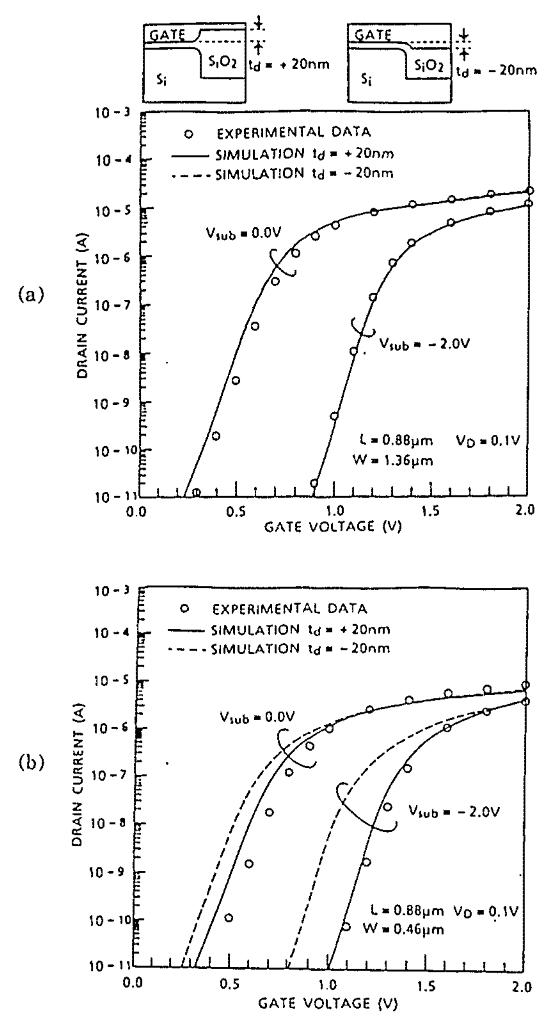


Fig.4 $I_D$ - $V_G$ characteristics for two kinds of trench corner shapes. The channel width are (a) 1.36μm and (b) 0.46μm respectively.