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FAST THREE-DIMENSIONAL PROCESS SIMULATION OF MOS DEVICES

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A 3D process simulation of an LDDMOS device has been performed using OPUS(1). The initial part of the processes including field oxidation, gate oxidation and boron implantation for Vt control is simulated rigorously in 2D space. Then, the 2D space is expanded into 3D space by shifting the 2D structure into z-direction as shown in fig.1. Gate polysilicon formation, phosphorus implantation for LDD, spacer formation and arsenic implantation for source/drain are simulated in 3D space.

Fig.2 shows a bird's eye view of the simulated nMOS LDD device. The number of cells is about 20,000. Active impurity concentration profiles at the silicon surface are shown through oxide and polysilicon. The drain junction is somewhat retarded toward channel region due to a 3D diffusion effect. Boron for channel stop diffuses out toward channel region, which causes Vt enhancement for narrower channel devices.

By replacing initial part of 3D simulations by 2D simulations, computation time is drastically reduced. Fig.3 compares CPU time of annealing in an inert ambient and ion implantation between 3D and 2D simulations. CPU time for 3D simulation is about 0.95(annealing) and 1.6(implantation) multiplied by the number of cells(Nz) in z-direction as much as that for 2D simulation. By assuming that CPU time ratio for moving boundary problems in 3D over 2D simulation is similar to that for ion implantation, CPU time of the current example by a full 3D process simulation is easily estimated. The result shows that CPU time by the current method is less than 10% than that by a full 3D simulation, showing the efficiency of this method.

(1):K.Nishi, K.Sakamoto, S.Kuroda, J.Ueda, T.Miyoshi and S.Ushio, IEEE Trans. Computer-Aided Design, vol.8, pp.675-683, 1989.

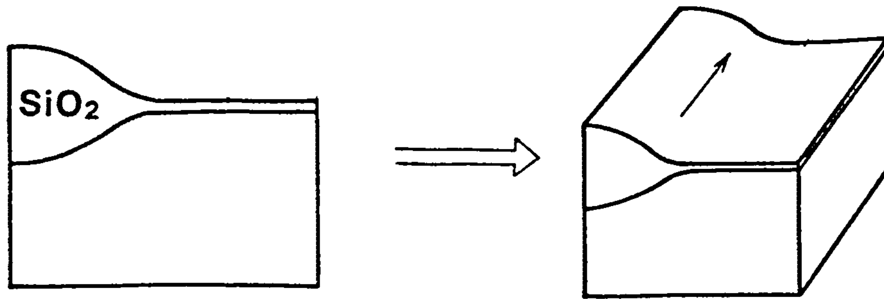

Fig.1:Example of SHIFT

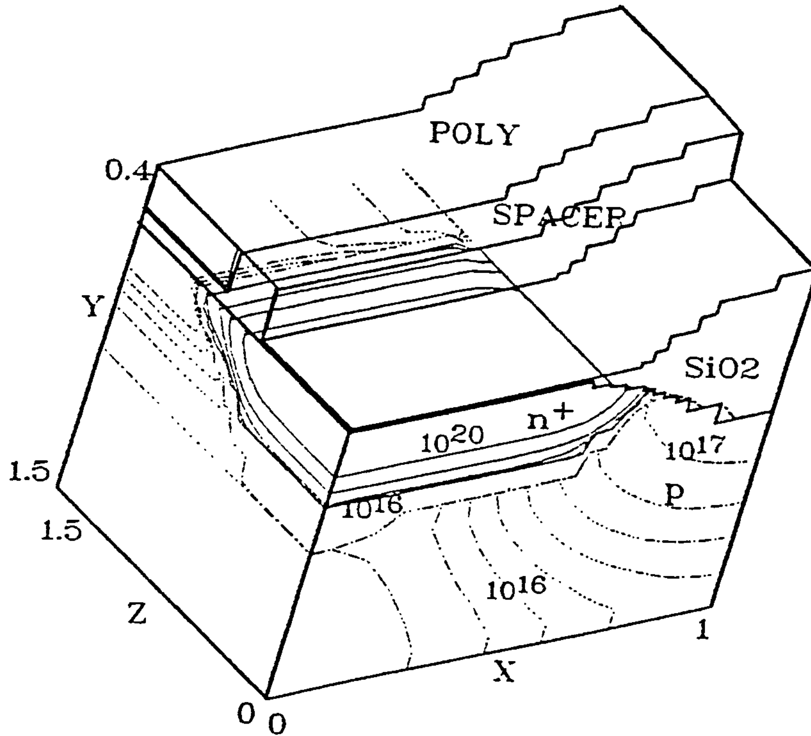

Fig.2:Bird's eye view of an LDDMOS device

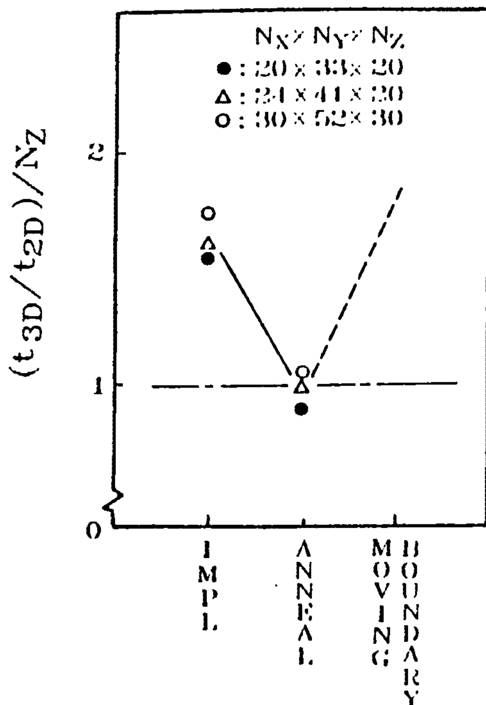

Fig.3:Comparison of the CPU time between 3D and 2D simulation