MOSFET SIMULATION WITH B-B TUNNEL CURRENT EFFECT

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ABSTRACT

Experimental observations on significant gate-induced drain leakage current are reported in thin gate oxide MOSFET at drain voltages much lower than the breakdown voltages[1], [2]. This current is attributed to the band-to-band tunneling occuring in the deep-depletion layer in the gate to drain overlap region. This tunneing current flows from drain to substrate, rather than to source.

When the MOS technology is scaled down to the deep submicron regime, this tunnel current becomes very important in high density and low power CMOS technologies such as DRAM, SRAM etc. In order to meet this type of leakage current, we incorporated this band-to-band tunnel current effect to the two dimensional device simulator and investigated the effect.

The field in silicon at the Si-SiO2 interface also depends on the doping concentrations in the diffusion region and the voltage difference between drain and gate. The surface field at the dominant tunneling current position can be expressed as

$$Es = \frac{Vg - Vd - \Psi s}{3Tox},$$

where Es is the surface field and Ψs is the deep-depleted surface potential and at the order of $\simeq$ 1.2V. To model the tunneling current, we apply the equation derived for reversed-biased p-n junction diode[3],

$$J = A\ Esi\ \exp(-B/Esi),$$

where Esi is the average junction field and A, B are the physical constants. Since the surface field is dominant, we make approximation Esi =Es and for A, B, appropriate values are chosen. The tunnel current effect is incorporated to the generation term and we investigated for the case of Si oxide thickness of Tox 80Å and for the channel length ℓ = 0.5μm.

The simultion was performed under the condition of Vs, Vg, Vsub = 0v, and Vd = 0 ~ 20v. The net impurity distribution is shown in Fig. 1. Shown in Fig. 2, and Fig. 3 are the potential and electric field respectively. Fig. 4 shows the flow of electron flux from substrate to drain and Fig. 5 shows the flow of the hole flux to substrate. These electrons and holes are generated in the deep depletion layer of the gate to drain overlap region. Drain current is plotted with drain voltage varied from 0 to 20V. For 10v drain voltage, tunneling current resulted in the order of 10^{-7} A, and 5 orders of magnitude larger than the case without tunnel current effect which agrees with the experimental observation[1], [2]. This leakage current becomes significant for the deep submicron ULSI and we might need to contrive the structure resistent to this kind of tunnel current effect.

REFERENCES

[1] C. Chang and J. Lien, 1987 IEDM Technical Digest, pp714-717.
[2] T. Y. Chan, J. Chen, P. K. Ko and Hu, 1987 IEDM Technical Digest, pp718-721.
[3] S. M. Moll, "Physics of Semiconductor Devices", 2nd edition, Wiley New York, P. 525, 1981.

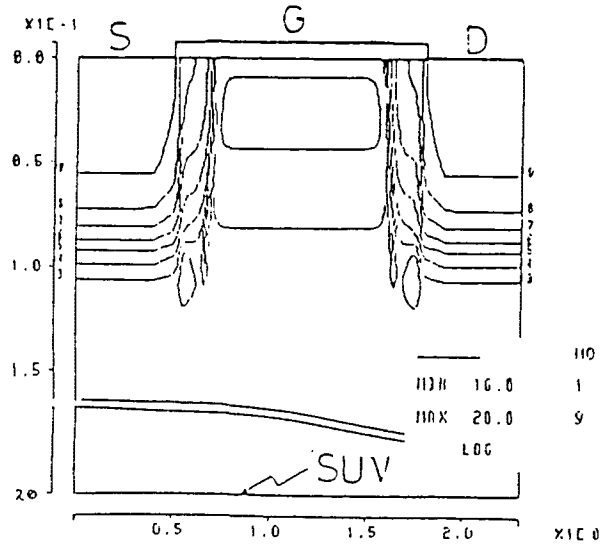

Fig. 1 contour of net impurity

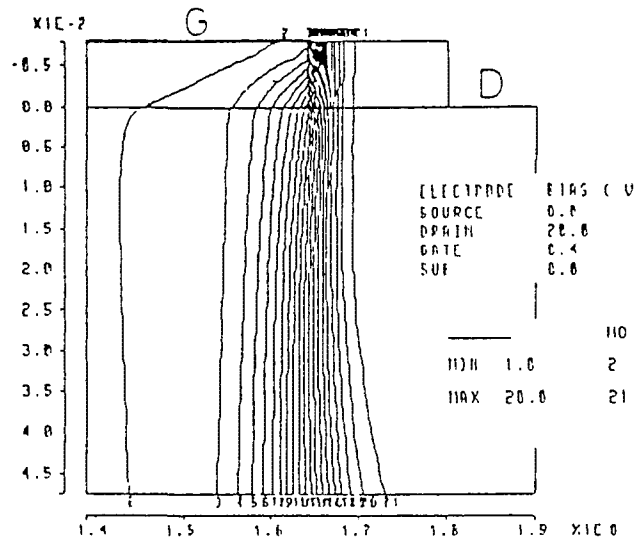

Fig. 2 contour of potential

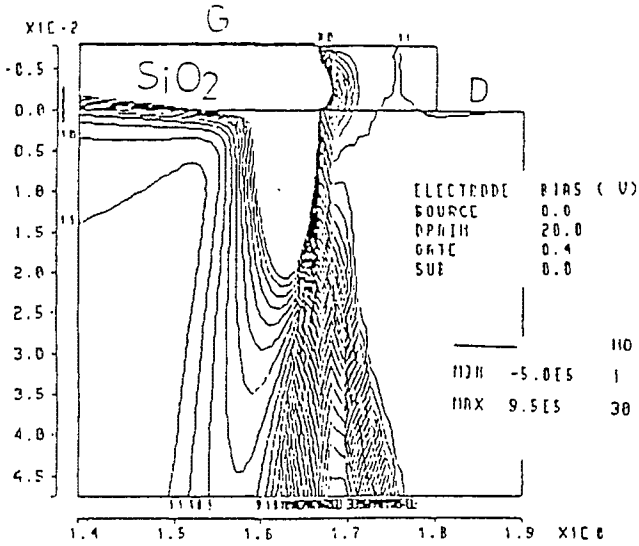

Fig. 3 contour of electric field (vertical component)

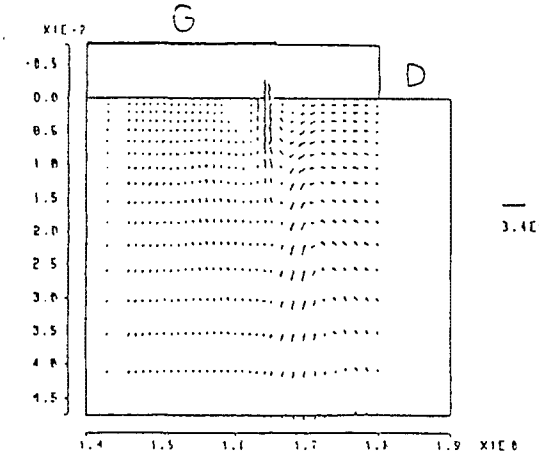

Fig. 4 vector of electron flux

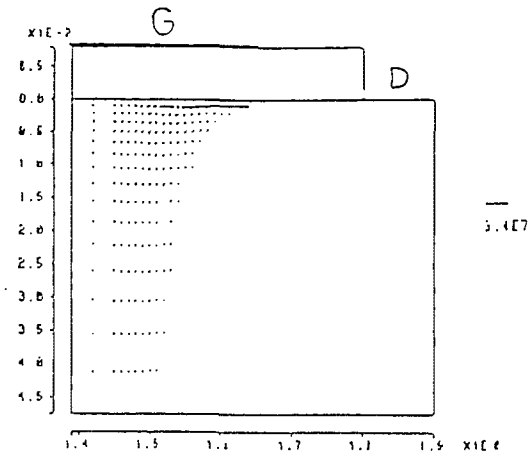

Fig. 5 vector of hole flux

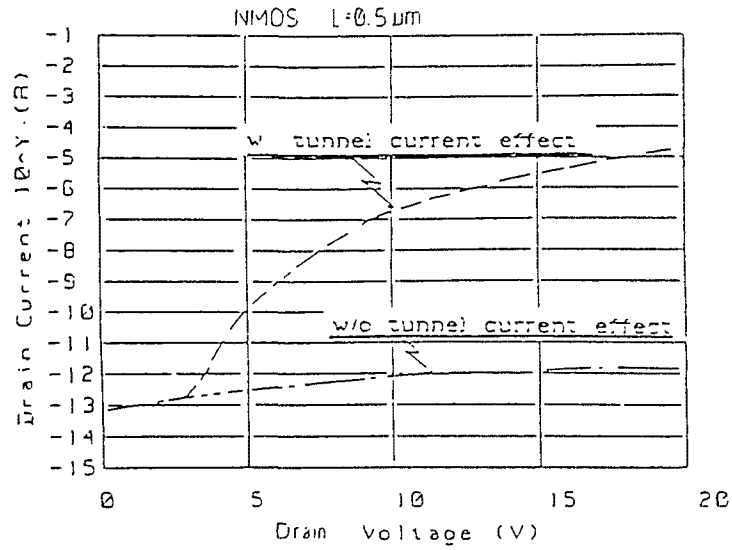

Fig. 6 drain current v.s. drain voltage