MOSTSM: MOS Transistor Sub-um Model for Circuit Simulation
- Basic I-V Model -

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Abstract

This paper describes a sub-um MOSFET model used as a circuit simulator. The object is to realize a simple model that gives good agreement with experimental result. To achieve this, we have developed (1) a novel formulation for carrier mobility degradation by a gate electric field and (2) a compact channel-length modulation model for MOSFET operation in the saturation region. A maximum I-V model error of 1%, in 0.6um NMOS devices is achieved.

1. MOSTSM Formulation

(a) Weak-inversion model

The following I-V model is used to describe MOSFET sub-threshold conduction.

$$I_{ds} = \beta^* * \left(1 - \exp\left(\frac{-V_d}{V_t}\right)\right) \exp\left(\frac{AV_e}{\beta^*}\right) \qquad (2.1)$$

$$\beta^* = \beta_0 \left(\frac{W}{L}\right) \frac{1}{A} \left(\frac{kT}{q}\right)^2 \qquad (2.2)$$

where, Vd is drain voltage, Vt ; threshold voltage, A ; sub-threshold slope coefficient, Ve ; effective gate voltage (=Vg - Vt), βo ; channel conductance of unit gate-area, W and L ; channel width and length, and (kT/q); Boltzmann voltage.

(b) Strong-inversion model

We employed simple I-V equations as shown below for the linear operational region:

$$I_{ds} = \frac{W}{L} \beta_{eff} \left(V_e - \frac{a}{2} V_d\right) V_d ; \qquad \text{Linear region} \qquad (2.3)$$

$$I_{ds} = \frac{I_{dsat}}{1 - (\delta L / L)} ; \qquad \text{Saturation region} \qquad (2.4)$$

Here, Idsat is saturation drain current, and parameter 'a' exhibits an effective depletion charge effect, which is formulated by.

$$a = 1 + \frac{K_{bo}}{2\sqrt{|V_b| + 2\phi_f}} \left(1 - \frac{1}{1.41 + 0.43(|V_b| + 2\phi_f)}\right) \qquad (2.5)$$

where, Kbo is substrate-bias constant, Vb; substrate-bias voltage, and ϕ_f; Fermi-potential.

In the saturation-region bias condition, the I-V curve is characterized by channel length modulation, 'δL'. we formulate the gate-field effect on the 'βeff' as;

$$\beta_e = \frac{\beta_o (\sqrt{\theta_{c1}} + \sqrt{\theta_{c2}})^2 V_e}{(1 + \theta_{c1} V_e)(1 + \theta_{c2} V_e)} \qquad (2.6)$$

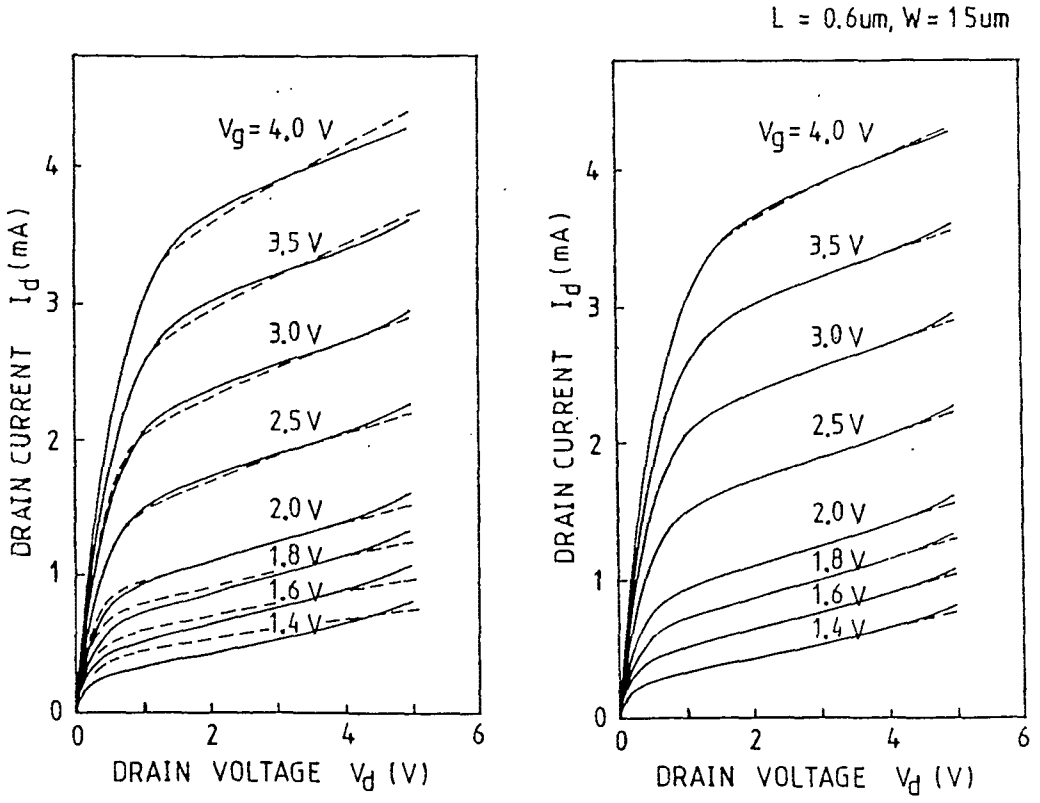
where, 'θe1' and 'θe2' indicate high and low gate field factors, respectively. It is noted that the bo has a unique value independent of device dimensions L and W (channel width).

2. EXPERIMENT

Figure 1 (a) shows an experimental comparison with a conventional MOSFET model which describes the gate field effects on 'βeff' by ;

$$\beta_{eff} = \frac{\beta_o}{1 + \theta(V_g - V_t)} \tag{3.1}$$

This equation shows monotonic decrease in 'βeff' as 'Vg' increases. As shown in the figure, the conventional model demonstrates better agreement with experiment at high gate bias. However, a large discrepancy is observed near the threshold gate bias condition. The MOSTSM model is compared with the experiment as shown in Fig.1 (b) , and excellent agreement with experiment is demonstrated.



(a) Conventional Model (b) MOSTSM Model

Fig.1 Experimental curve fitting based on the conventional and MOSTSM model at low current bias condition. (solid line: experiment, dashed line: model)