

Device Modeling of GaAs MESFETs for LSI:
Importance of Acceptors in the Semi-insulating Substrate

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GaAs MESFETs fabricated on the semi-insulating substrate are now very important devices to realize high-speed LSI. The MESFETs characteristics strongly depend on junction properties between the active layer and the substrate. This is because a semi-insulating material is achieved by impurity compensation by deep levels. However, most of the numerical models have neglected this impurity compensation[1]. In this report, we present numerical simulations of GaAs MESFETs on various types of substrates that include deep levels, and demonstrate the importance of this effect in the modeling of MESFETs.

The device structure simulated here is shown in Fig.1. We consider three types of substrates: 1)undoped semi-insulating LEC GaAs, where deep donors "EL2"(N_{EL2}) compensate shallow acceptors(N_{Ai}), 2)a substrate with a p-buffer layer on the undoped LEC GaAs, 3)Cr-doped semi-insulating substrate, where deep acceptors "Cr"(N_{Cr}) compensate shallow donors(N_{Di}). A two-carrier simulation is made because deep levels are included.

Fig.2 shows drain characteristics of 0.3 μm gate-length MESFETs on the substrate including deep donors "EL2" or deep acceptors "Cr". Three features are observed. (1)The drain currents increase continuously with drain voltage, particularly for a case with lower N_{Ai} or N_{Cr} . (2)The drain currents are lower for higher N_{Ai} or N_{Cr} . (3)The drain currents are determined by acceptor density in the substrate, whether the acceptor is shallow or deep. The unsaturation of drain currents can be explained by the presence of substrate conduction, which exists because electrons are injected to fill the traps in the substrate. The dependence of drain characteristics on N_{Ai} or N_{Cr} can be understood by considering the formation of space-charge layer. For higher N_{Ai} or N_{Cr} , the barrier at the active layer-substrate interface is steeper due to higher density of negative charges in the substrate, resulting in lower substrate current. As mentioned in (3), the drain currents are determined by N_{Ai} or N_{Cr} . However, potential profiles depend on the nature of deep levels, as shown in Fig.3, suggesting that different drain breakdown characteristics or backgating effects may be observed between the two cases.

Fig.4 shows the threshold voltage V_{Th} versus gate length L_G , with the thickness of a p-buffer layer d as a parameter[2]. For thinner d , V_{Th} shift with shortening the gate length is larger. This arises from the increase in the direct substrate current with shortening the gate length. It is concluded that using a thick p-buffer layer has the same effect as using a substrate with high density of traps in the point that both of them minimize the short-channel effect. Fig.5 shows V_{Th} - L_G curves for the case with the deep acceptors "Cr", indicating that for higher deep-acceptor density, the short-channel effect is reduced, too.

In conclusion, the acceptor density in the substrate is a very important factor to determine I-V characteristics, whether the acceptor is shallow or deep. Therefore, impurity compensation by deep levels must be considered in the modeling of GaAs MESFETs. It is demonstrated that the acceptor density in the semi-insulating substrate must be made high to minimize the short-channel effects in GaAs MESFETs.

[1] K.Horio et al., IEEE Trans. Electron Devices, vol.ED-35, pp.1778-1785 (1988).

[2] K.Horio et al., to be published in IEEE Trans. Microwave Theory Tech., vol.MTT-37, no.9 (1989).

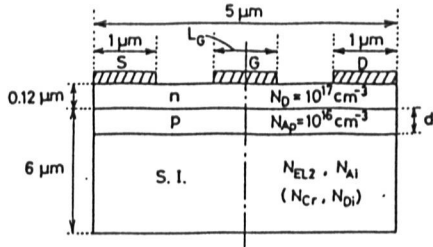


Fig.1 Modeled GaAs MESFET (with a p-buffer layer) on the semi-insulating substrate compensated by deep levels.

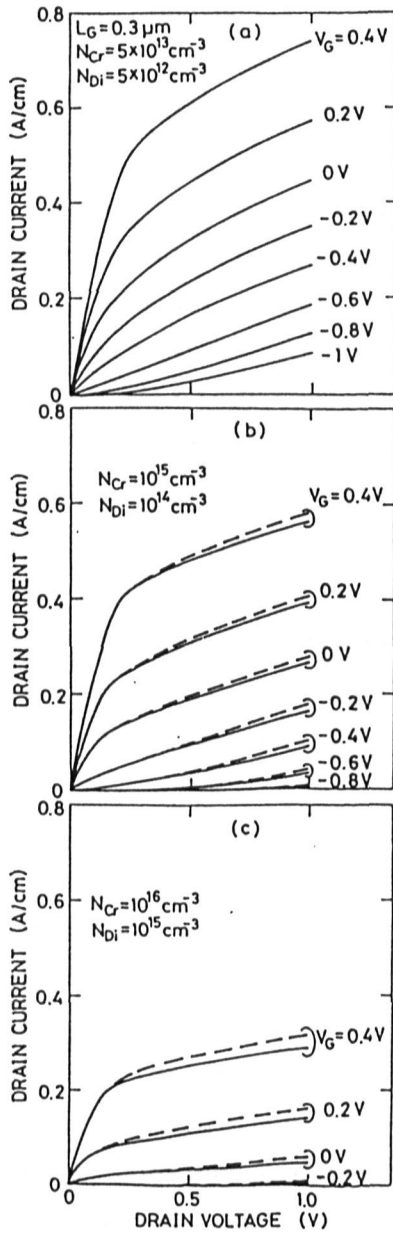


Fig.2 Calculated drain characteristics of 0.3 μm gate-length GaAs MESFETs on the substrate including deep acceptors "Cr" (solid lines). The dashed lines correspond to the case with a substrate including deep donors "EL2" in which $N_{Ai}/N_{EL2} = 0.1$. N_{Ai} is set to equal N_{Cr} in respective figures. $d = 0$ μm.

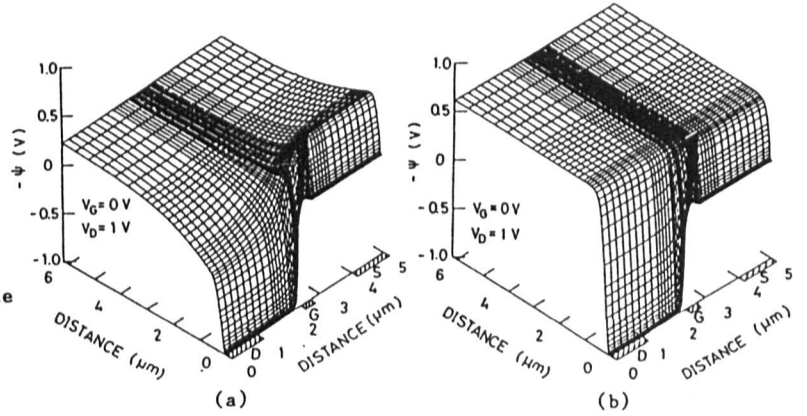


Fig.3 Comparison of potential profiles of 0.3 μm gate-length GaAs MESFETs with different types of substrates. $V_G = 0$ V and $V_D = 1$ V. (a) Substrate with deep donors "EL2" ($N_{EL2} = 10^{17}$ cm⁻³, $N_{Ai} = 10^{16}$ cm⁻³). (b) Substrate with deep acceptors "Cr" ($N_{Cr} = 10^{16}$ cm⁻³, $N_{Di} = 10^{15}$ cm⁻³).

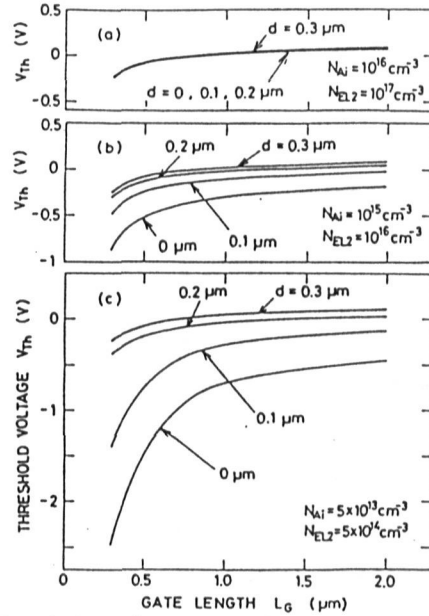


Fig.4 Threshold voltage as a function of gate length for GaAs MESFETs with a p-buffer layer on the substrate including deep donors "EL2". Three cases with different N_{Ai} and N_{EL2} are shown.

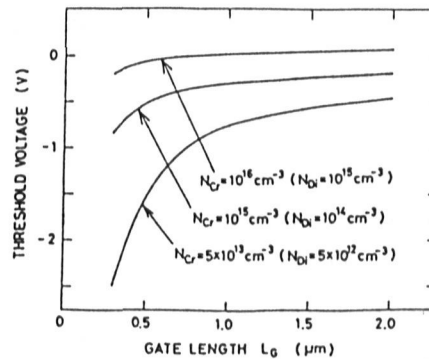


Fig.5 Threshold voltage as a function of gate length for GaAs MESFETs on the substrate including deep acceptors "Cr", with N_{Cr} and N_{Di} as parameters.