

EXAMINATION OF BOUNDARY LOCATION INFLUENCE ON PERIODIC WIRING CAPACITANCE SIMULATION

Sanae FUKUDA, Naoyuki SHIGYO and Koichi KATO

ULSI Research Center, Toshiba Corporation
1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

The influence of the boundary location on periodic wiring capacitance simulation has been investigated. The wiring capacitances were calculated by solving Laplace's equation in the simulation. The Dirichlet type boundary conditions were set for the electrodes, and the Neumann type for the symmetric planes. The wiring patterns used in VLSI are periodic, hence simulation is usually performed using the calculation region shown in Fig. 1 (a), where the Neumann boundary plane is placed at the center of an *electrode* (E_2 type). However, we have found that the wiring capacitance depended strongly on the boundary location. When the Neumann boundary plane is placed at the center of an *insulator* (I_2 type), as shown in Fig. 1 (b), the simulated capacitance value results in a large difference compared with the one for the E_2 type.

Figure 2 (a) shows the calculation regions for an I_n type, where the number of including electrodes n is a parameter. The simulated capacitances for I_n are shown in Fig. 2 (b). The capacitance values depend strongly on the calculation regions. Comparison of the simulated $C_{1,2}$ values for I_2 and I_5 resulted in a 15.2 percent difference. In addition, $C_{2,3}$ did not coincide with $C_{1,2}$ for I_4 and I_5 .

The above dependency is explained as follows. Due to the Neumann boundary condition employed for the side planes, the equivalent applied bias for the I_2 type is as shown in Fig. 3. Hence, the simulated capacitance for the I_2 type is expressed by the following equation.

$$\begin{aligned} C_{1,2}^{I_2} &= C_{1,2}^* + C_{1,3}^* + C_{1,-2}^* + C_{1,-3}^* + C_{1,6}^* + C_{1,7}^* + \dots \\ &= C_{1,2}^* + 2C_{1,3}^* + C_{1,4}^* + \sum_{j=1}^{+\infty} (C_{1,4j+2}^* + 2C_{1,4j+3}^* + C_{1,4j+4}^*) \end{aligned} \quad (1)$$

where the superscript * means the true capacitance. $C_{1,2}^{I_2}$ is not equal to $C_{1,2}^*$. This discrepancy originates from the additional charge induced by the electrodes except electrode 2 due to the Neumann boundary condition. The simulation always overestimated the capacitance value. The same explanation is applicable to the E_2 type, and the capacitance is given as

$$C_{1,2}^{E_2} = C_{1,2}^* + \sum_{j=1}^{+\infty} C_{1,2j+2}^* \quad (2)$$

The general expressions of $C_{1,2}$ for I_n and E_n ($n \geq 3$) are obtained as follows.

$$C_{1,2}^{I_n} = C_{1,2}^* + C_{1,3}^* + \sum_{j=1}^{+\infty} (C_{1,2nj-1}^* + C_{1,2nj}^* + C_{1,2nj+2}^* + C_{1,2nj+3}^*) \quad (3)$$

$$C_{1,2}^{E_n} = C_{1,2}^* + \sum_{j=1}^{+\infty} (C_{1,2(n-1)j}^* + C_{1,2(n-1)j+2}^*) \quad (4)$$

In previous works [1]-[3], excellent agreements between measurements and simulations have been reported. The typical wiring pattern layout for the measurements has been periodic, as shown in Fig. 4. This measurement corresponds to an E_2 type simulation. Hence, the measured capacitance values agree well with the simulation of the E_2 type. However, this measured capacitance also involves the same error as (2).

In summary, the influence of the boundary location on periodic wiring capacitance simulation has been examined. The dependence of the capacitance values on the calculation region originates from the additional charge induced by the unexpectedly biased electrodes due to the Neumann boundary condition. It should be noted that measurements with a periodic wiring pattern also involve an error due to the periodic nature of the wiring.

References

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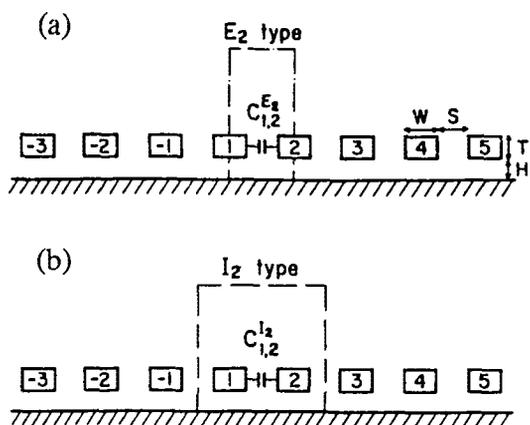


Fig. 1 Boundary conditions for periodic wirings.

- (a) E₂ type : Neumann boundary plane is placed at the center of the electrode.
- (b) I₂ type : Neumann boundary plane is placed at the center of the insulator between neighboring electrodes.

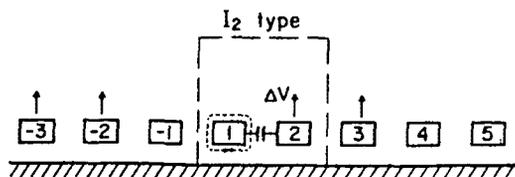


Fig. 3 Explanation of the dependency on I₂ type boundary condition. Induced charge Q₁ is calculated by integrating the electric field around electrode 1 as indicated by the dashed line.

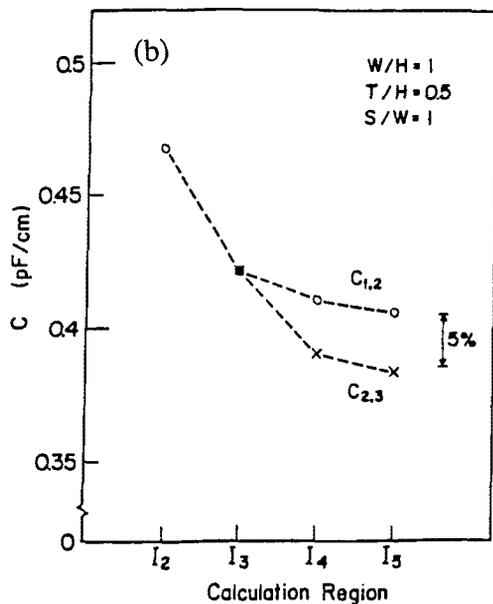
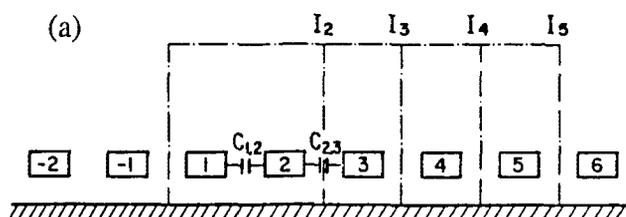


Fig. 2 (a) Calculation regions for I_n type (b) its influence on simulated capacitances.

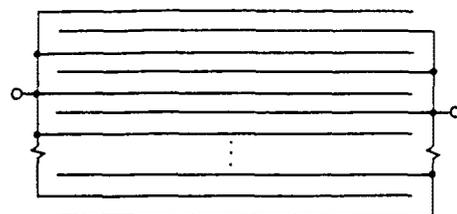


Fig. 4 Wiring pattern for measurement.