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BOUNDARY CONDITIONS IN MIXED-MODE DEVICE SIMULATION

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Boundary conditions are key to all aspects of Technology CAD. For process modeling the role of surfaces on point defect concentrations and impurity segregation fluxes is critical. At the circuit/device level there is a range of problems. Transient circuit boundary conditions control many device level device problems such as latchup, electro-static discharge and other bipolar effects. The growing importance of mixed-mode simulation is now apparent. This paper deals specifically with the boundary conditions between drift/diffusion(D/D) and Monte Carlo(MC) device simulators.

The use of windowed MC analysis has been proposed as a means to exploit the accuracy of MC analysis while limiting the extent of the analysis domain to conserve CPU time. However the technique requires careful window placement to avoid nonphysical effects. The use of D/D analysis to provide initial conditions and to help properly specify boundary conditions is discussed. Figure 1 shows a sub-0.1μm GaAs device which exploits gate trench and highly doped capping layer to achieve excellent current-voltage characteristics. Figure 2 shows the comparison of D/D analysis of the complete device and a simplified drain contact where the length L_{CE} is specified to give equal drain current. As can be seen from the comparison of Figures 2(c) and (d), the potential contours are virtually identical. Based on such specification of drain contact, the analysis shown in Figure 3 results. Here the experimental results are compared with windowed MC based on two boundary specifications. The lower set of simulations (labeled $L_{FG}+L_{GH}$) correspond to using an equivalent length taken as the sum of the actual contact height and length. The upper set of simulation results (labeled L_{CE}) correspond to a MC contact window calculated based on the D/D solution corresponding to that in Figure 2(d).

The above discussion emphasizes the windowing aspects of mixed-mode D/D-MC analysis. Also discussed is the use of parallel computation techniques to achieve the MC analysis. Figure 4 shows a simple schematic diagram of the partitioning of MC simulation over parallel CPUs. Based on results for several computer architectures, a linear speed-up with number of processors has been demonstrated up to 20 CPUs.

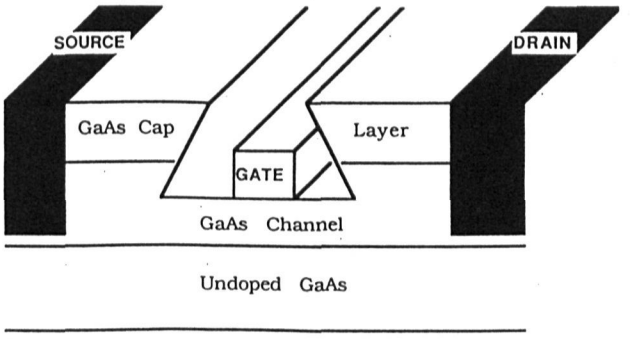

Fig. 1 Device structure of two sub-0.1 μm GaAs MESFET's.

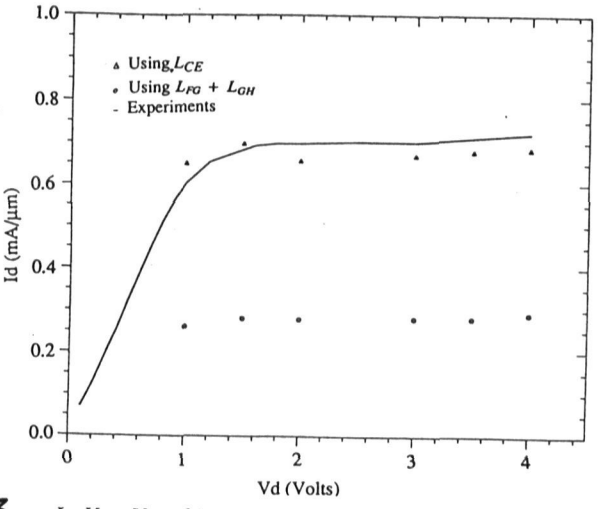

Fig. 3 I_d–V_d at $V_g = 0$ V using drain contact length $L_{FG} + L_{GH}$, and L_{CE} compared with the measured data.

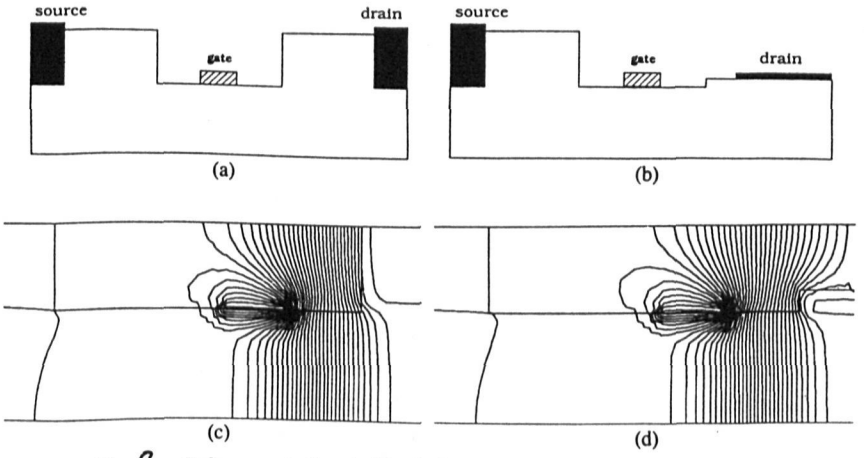

Fig. 2 Enforcement of equivalent drain current collection is reasonable. (a) and (b) are two simulation domains. (c) and (d) are equipotential contours of the PISCES results.

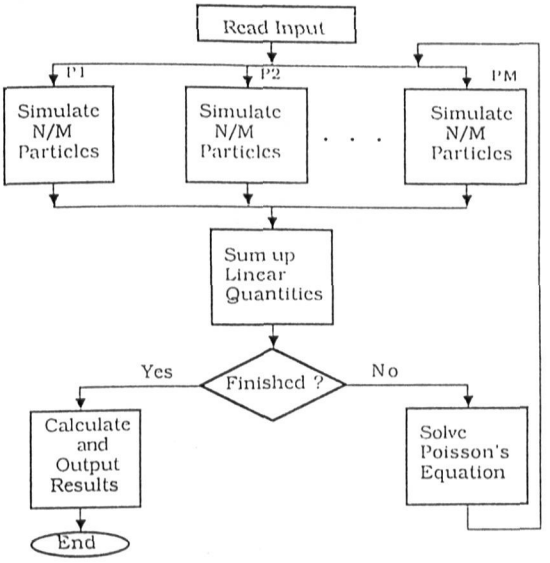

Fig. 4 Flowchart of the McPOP program.