11:30-11:45 [9]

3D Analysis for Wiring Capacitance with Finite Element Method

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Abstract

With the reduction of device size to realize high speed and high packing density, the wiring-related parasitic elements such as capacitances and resistances become effective in device performance. In this work, a three-dimensional finite element method, which is capable to include the arbitrary wiring placements, has been applied to the evaluation of wiring capacitances and resistances, in comparison with two-dimensional and one-dimensional simulations.

The electric field on each wire is calculated based on the 3D Laplace equation and the charge can be derived based on the Gauss theorem. From the charge distribution, total and mutual wiring capacitance are obtained. Moreover, the wiring resistance is calculated by only replacing the dielectric constant with the inverse of the conductivity in the same manner. Through this process, the equation is discretized by the finite element method, in which the volume co-ordinates in the arbitrary elements is applied as the weighted-function. Successively, the matrix is solved using the BCG method.

Two types of wiring pattern are assumed as indicated in Fig.1. The potential distribution for A pattern is calculated, as shown in Fig.2. It can be seen from the figure that the peripheral effects come out. Figure 3 demonstrates the mutual capacitance for the A pattern in Fig.1 divided by one-dimensional calculation with a parameter of vertical size H, line width, W and the distance between two lines, T, in comparison with two-dimensional calculation. With the reduction of H/W, the peripheral effects become dominant. Similarly, Fig.4 shows the mutual capacitance for the B pattern in Fig.1. These figures suggest that the A pattern is more effective in peripheral effects as can be estimated.

Thus, the present simulator becomes an indispensable tool for designing the wiring in VLSI. After this, it is important to develop more user-friendly input and output interface.

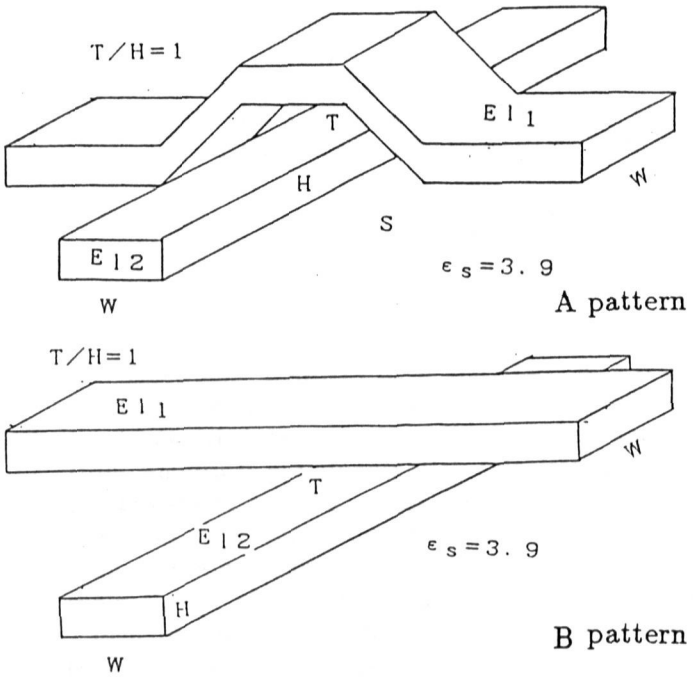

Fig.1. Two-types of wiring pattern.

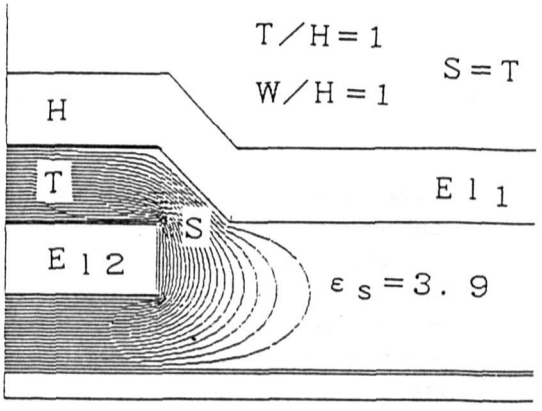

Fig.2. Potential distribution for A pattern

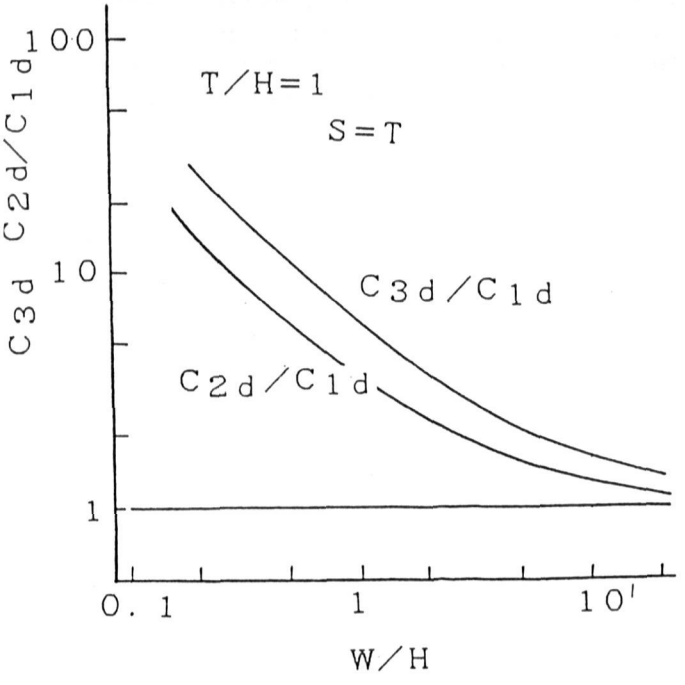

Fig.3. Mutual capacitance vs. W/H for A pattern.

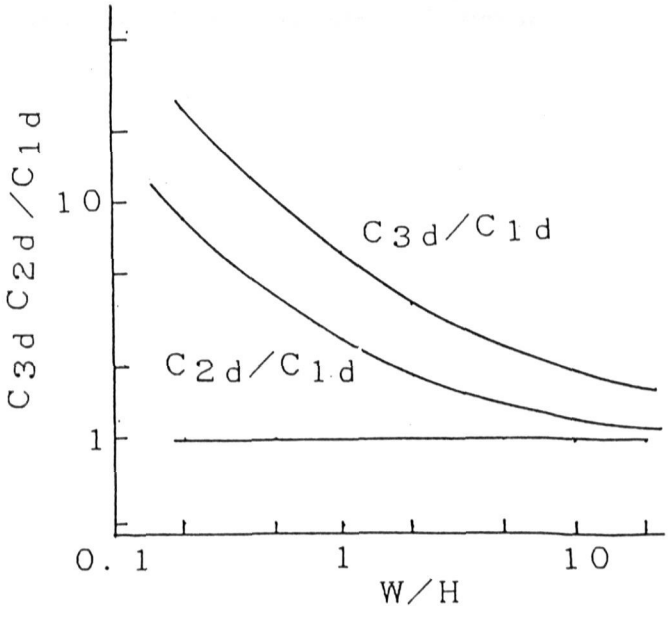

Fig.4. Mutual capacitance vs. W/H for B pattern.