A Completely Physically Based MOSFET Model Focusing on Channel Shortening Effects for Circuit Design

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ABSTRACT

This paper is about a physically based MOS model for VLSI circuit simulation that considers geometry (channel length) effects. A simple analytical MOS model is proposed that is correct for all transistor operation regions. The model newly includes the geometry effects on substrate bias effects of V_{TH} and two-dimensional field effects on channel conductance β. The results of its application to 0.8 μm MOS devices show excellent agreement with data on measured devices: the average error is only 0.5 %. This model has been used for a year in the actual design of MOS analog circuits, EEPROMs and gate arrays.

1. INTRODUCTION.

Many geometry-dependent models (L, W) [1][2] have been proposed for MOS LSI statistical circuit design. All the models, however, have empirical equations, which requires experimental parameter extractions, resulting in a model parameter database, before using them. Furthermore, none of the conventional model parameter equations, e.g. $\alpha_1/L+\alpha_2/L^2$, is found to be sufficient for accurate modeling. Our final goal of MOS model is simple and completely physically based model equations and its parameters. The features of the model proposed are:

1) valid over all regions of MOSFET operations.
2) physically based geometry (L_{eff}) effects which describe the key model parameters, V_{TH}, K and β.
3) a continuous conductance among various operational regions.

2. MODEL EQUATIONS.

We employed a basic equations with a simple form as shown in the Table 1. Sub-threshold operation is modeled using linear combination of both equations on weak and strong inversion models, to achieve a smooth transition between them. Channel length effects are focused on threshold voltage (V_{TH}) and channel conductance (β) modeling as a parameters with drain and gate field.

First, the threshold voltage and back gate constant (K_B) are most sensitive device parameters, which is affected by geometry for submicron short channel MOSFETs. A two-dimensional device simulation model [3] was employed to determine the physical equations leading to $V_{TH}(L)$ and $K_B(L)$ in exponential forms. It is as follows.

$$V_{TH}=V_{T0}+K_B(\sqrt{2\varphi_F+V_B}-\sqrt{2\varphi_F})-K_DV_D \quad (1)$$

where V_{T0}, K_B and K_D are the original model parameters. Their channel length dependences are shown in Fig. 1 and they are expressed as follows:

$$V_{T0}=V_{TL}-\eta_0 exp(-L_{eff}/l_0) \quad (2)$$

$$K_B=K_{BL}-\eta_B exp(-L_{eff}/l_B) \quad (3)$$

$$K_D=K_{DL}/L_{eff}^3 \quad (4)$$

where V_{TL}, η_0, l_0, K_{BL}, η_B, l_B and K_{DL} are kept as new model parameters.

Second, to describe the geometry effects on β, we introduced new understandings on gate field model. Fig. 2 shows an typical β-V_{GS} curves of a 0.8 μm MOS device. As shown in Fig. 2, it shows a large L_{eff} dependency. To explain this phenomena, let's assume a simple gradual channel model to derive horizontal channel field at source edge. At saturation conditions, I_{DS} is described as

Table 1 New Model

Channel-Dependent Drain Current Model
$\cdot I_D=\frac{W}{L-\Delta L}\cdot\beta(V_D,V_G)\cdot(Ve-aV_D/2)\cdot V_D$
$\cdot I_{tail}=\beta\cdot exp(AV_G/Vt)\cdot[1-exp(V_D/Vt)]$
Features:
1) Applicability to all bias regions [4] (from the sub-threshold to saturation regions).
2) Applicable to short channel MOSFETs
a) velocity saturation effect, $\beta=\beta(V_D)$,
b) V_G mobility dependence, $\beta=\beta(V_G)$,
c) channel modulation effect, $\Delta L\neq 0$.
3) Physical model.

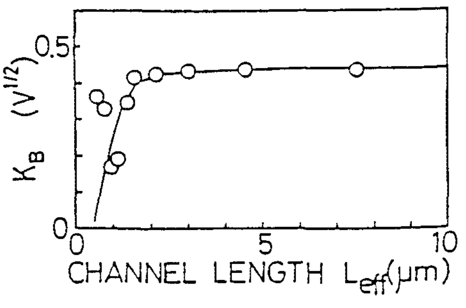

Fig. 1 Dependence of original model parameters on channel length. -:model, O:extracted results from experimental data.

$$I_{DS}=\frac{1}{2}C_{OX}\frac{W}{L_{eff}}\mu_n V_{GS}^2 \qquad (5)$$

On the other hand. I_{DS} at source edge is expressed in another form by

$$I_{DS}=nq\mu_n\frac{\partial\phi_s}{\partial x}\bigg|_{x=0}=W\mu C_{OX}V_G\frac{\partial\phi_s}{\partial x}\bigg|_{x=0} \qquad (6)$$

Therefore. from Eq. 5 and 6. the channel field is simply derived as

$$\frac{\partial\phi_s}{\partial x}\bigg|_{x=0}=\frac{V_G}{2L} \qquad (7)$$

To think about the critical field for electron velocity saturation of E_{crit}~10 kV/cm the critical channel length at V_G=5 V is estimated to be 5 μm. Therefore. it is understood that large L_{eff} dependency on β-V_{GS} characteristics is due to carrier velocity saturation "at the source edge". We found that a simple formula of L^{-1} is sufficient to express β degradation.

3. APPLICATIONS and DISCUSSIONS.

The model was used on 0.8 μm MOS devices with oxide thickness of 20 nm and n^+ junction depth of 0.2 μm to verify its accuracy. The results show good matching between modeled and measured data for devices with an L_{eff}=0.7~1.5 μm. as presented in Fig. 3. The average error for these five devices was only 0.5 %. Extraction of the new model parameters was done by using 1 to 3 device characteristics on a main-frame with an automatic parameter extraction system.

The error of the 0.5 μm devices in Fig. 3 resulted from deep punch-through between the source and drain. which the new model does not consider. Nevertheless. the model can be used for 0.5 μm devices if punch-through does not occurs.

The new model was implemented to a circuit simulator. in such a way that user can simply define "L" value in the input data. Therefore. once the channel dependence parameters are extracted. user can estimate easily the "L" dependent circuit performances by changing a single line in input data.

This model has been used for one year to design such things as analog circuits. EEPROMs. gate arrays and Mega-bits memories.

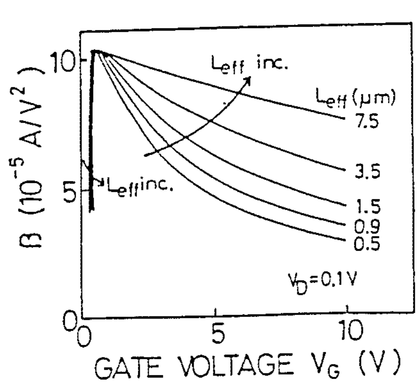

Fig. 2 Dependence of channel conductance. β. on V_G.

4. CONCLUSIONS.

A new MOSFET model has been developed. The features of this model are that:

(1) correct over all transistor operations;
(2) fully physically based model equations and parameters;
(3) accurate enough for sub-μm VLSI design with 0.5 % average error on I-V curves.

The model accuracy was confirmed through comparison with experimental data. This model can be utilized for various types of MOS LSI designing. for example. statistical design and a VLSI parameter shrink design considering channel length variations.

ACKNOWLEDGMENTS.

The authors wish to thank Masaaki AOKI and Kyoko ISHII for their measurements of the I-V data and Dr. Shojiro ASAI for his encouragement.

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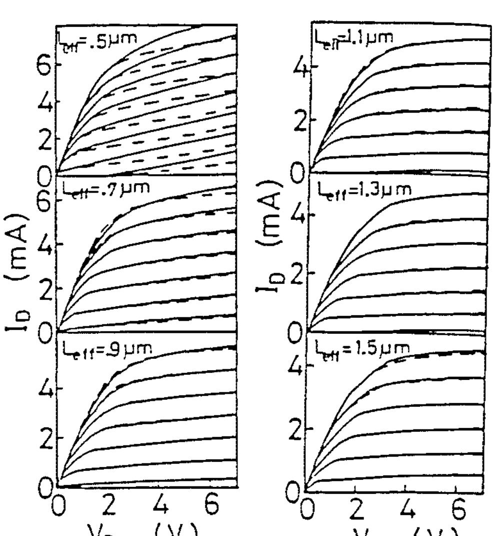

Fig. 3 I-V curves for nMOSFETs. Only one set of model parameters was needed to calculate the I-V curves for these six devices.
—:model. --:measured data. V_G=0~7V.