10:15-10:45 **[5]**

T O S H I E

A Table Generator for MOS Circuit Simulation

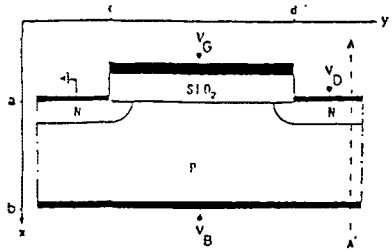
Karl Michael Eickhoff
Walter L. Engl
Institut für Theoretische Elektrotechnik
University of Aachen
Kopernikusstr. 16, D 5100 Aachen, West Germany

TOSHIE is a device modeling system for MOS circuit simulation. It incorporates an MOS Table Model for transient simulations with the MEDUSA circuit simulator and a Table Generator for the computation of the required data tables.

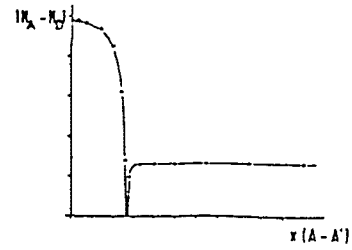
The objective of the Table Generator is to provide the data tables for the Table Model. The kernel of the Table Generator consists of an efficient 2D MOS device simulator. With this model, DC device simulations are carried out for a grid of transistor bias points. The resulting terminal currents and charges populate the transistor model data tables. The tables are automatically refined until user predefined accuracy of the model is obtained. For all MOS transistors of different channel lenght, an individual set of tables is computed and stored in the Model Library.

The Table Model, which is available in the circuit simulator MEDUSA, is fed with the required data tables from the Model Library. For a given set of terminal voltages, the Table Model computes DC and transient transistor terminal currents by table look-up techniques and interpolation between stored data values.

With the TOSHIE system, MOS circuits with more than 5,000 transistors - a 32 bit ALU as well as the critical path of a memory chip - were simulated on a Data General MV/10000 minicomputer.



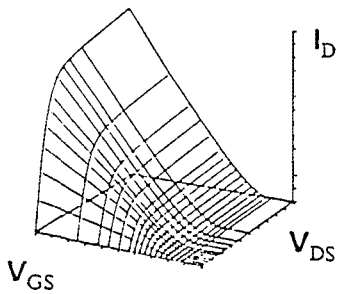
Geometry



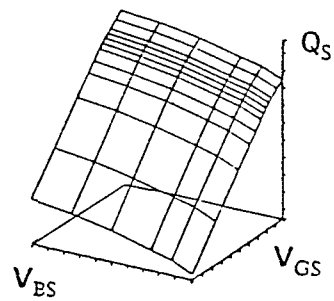
Doping

TOSHIE

Table Generator

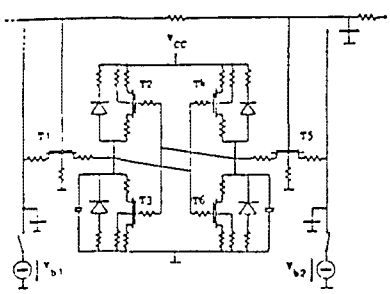


Current Table



Charge Tables

Model Library

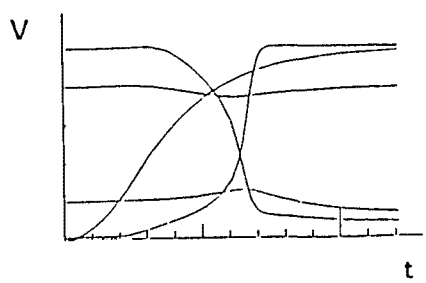


Circuit

MEDUSA

Numerical Model

Table Model



Waveforms

SYSTEM OVERVIEW