# COUPLED 2D PROCESS/DEVICE MODELS FOR SCALED MOS DEVICE

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Abstract

Coupled process simulation and device analysis is essential for submicron device design. There are a growing number of applications where the importance of advanced 2D models can be demonstrated. This paper emphasizes two themes--diffusion kinetics and hot electron effects. The modeling of diffusion has reached a new point of understanding and need for new data. From the known features of point defects at low concentrations we are now moving into the more complex area of high concentration point defect models. Recent simulations and modeling for source/drain doping profiles are discussed. Modeling of hot electron effects is critical for submicron technology. A new avalanche generation model suitable for implementation in the PISCES 2B simulator is discussed. Using Monte Carlo simulations to determine model parameters, the new model gives excellent agreement with both substrate current and even breakdown characteristics of short channel MOSFET. Importance of accurate modeling of mobility and contact resistance is discussed.

Accurate profile modeling in 2D is of growing importance as devices scale into the submicron regime. Progress in 2D modeling of both oxide shapes and junction profiles is reported. In the area of oxidation, the importance of including stress in modeling growth of thin oxides at low temperatures is essential. Applying the Eyring model as proposed by Sutardja provide a correct physical representation. Using this formulation and coefficients recently extracted by Rafferty, accurate modeling of corner effects such as shown in Figure 1 are now possible. These results show the oxide thinning at a trench corner. The shaded regions show contours of electric field, indicating a peak field strength of 1450 V/μm which can cause serious reliability problems.

The problems of modeling 2D diffusion, or even 1D for that matter, have persisted for more than two decades. Recent progress in low concentration intrinsic diffusion due to boundary condition effects such as oxidation nitridation and oxynitridation has been substantial--even for 2D effects. However, the modeling of high concentration extrinsic diffusion has been largely unsolved. Figure 2 shows the cross-section of a complex MOSFET structure which uses a JFET at the drain to avoid surface hot carrier effects. This figure shows SUPREM 4 simulations. Figure 3 shows PISCES electrical results based on 1D SUPREM 3 approximations to the profiles shown in Figure 2 and experimental results. The agreement is only marginal to poor. Figure 3 also shows the PISCES results and experiment, this time using the SUPREM 4 simulated profiles. The results are much improved showing the importance of having accurate profiles. Also, in order to get a good fit over the entire bias range, it was necessary to use the correct field dependent mobility data as reported by Watt.

The above results clearly illustrate the importance of having accurate profiles in modeling short channel devices. In addition to the role of accurate mobility modeling, hot electrons play an important role in performance characteristics of submicron devices. Several approaches have been proposed for hot carrier modeling including: Monte Carlo (MC) analysis, hydrodynamic models and analytic post processing based on drift/diffusion solutions. In this work we use a new avalanche generation model in PISCES (drift/diffusion) with parameters taken from MC analysis. Using hot carrier information determined from MC windowed simulations, a simple expression for mean free path as a function of device geometry and bias conditions is implemented as follows:

$$\lambda_{eff}=\lambda_o(L_{eff})\, e^{-V_o/K}$$

Figure 4 shows a plot of the effective mean free path as a function of bias levels and device geometry (conventional and LDD devices). The dependencies reflect physical trends related to shifts in peak electric field due to both doping and bias effects.

Based on the above model, PISCES can accurately predict substrate currents as shown in Figure 5. Here the currents are accurately predicted over the complete bias range for several bias conditions. In addition to the substrate current prediction, the new model gives accurate results for breakdown characteristics as shown in Figure 6. Here it is important to accurately model series resistance.

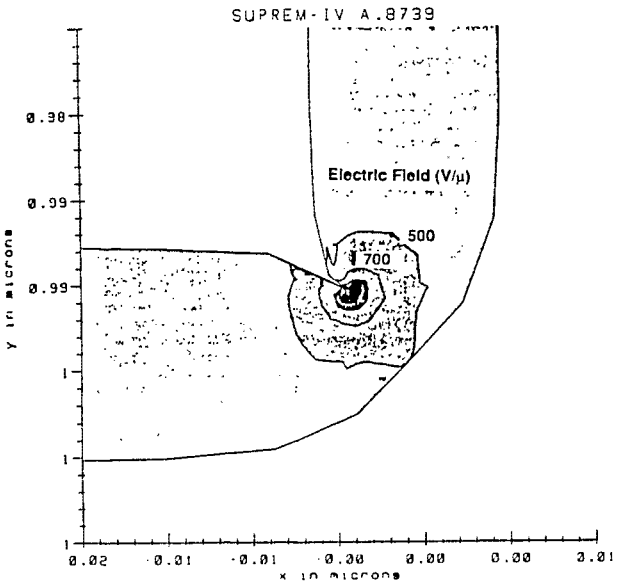


Fig. 1: SUPREM 4 simulation of trench corner oxidation. Electric field calculation obtained from coupled PISCES simulation.

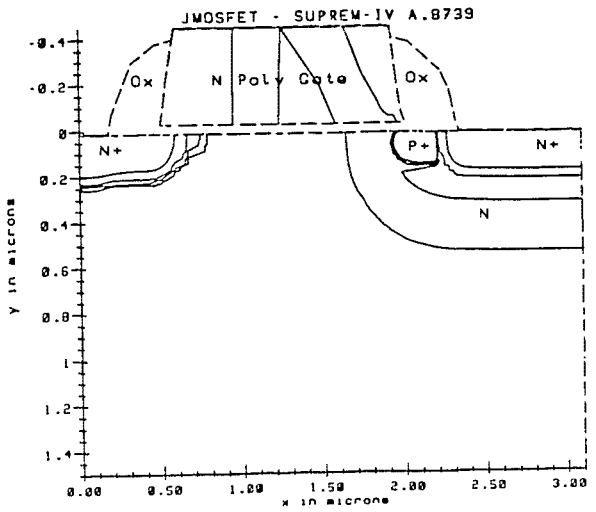


Fig. 2: Device cross-section of JMOS device as simulated with SUPREM 4

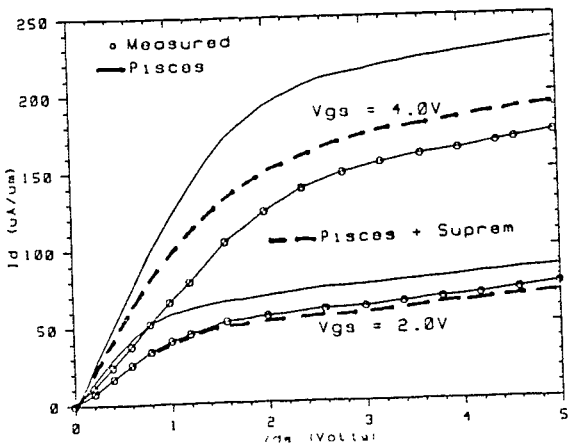


Fig. 3: Simulated and Measured JMOS device characteristics. (Solid line PISCES + SUPREM 3, dashed line PISCES + SUPREM 4)

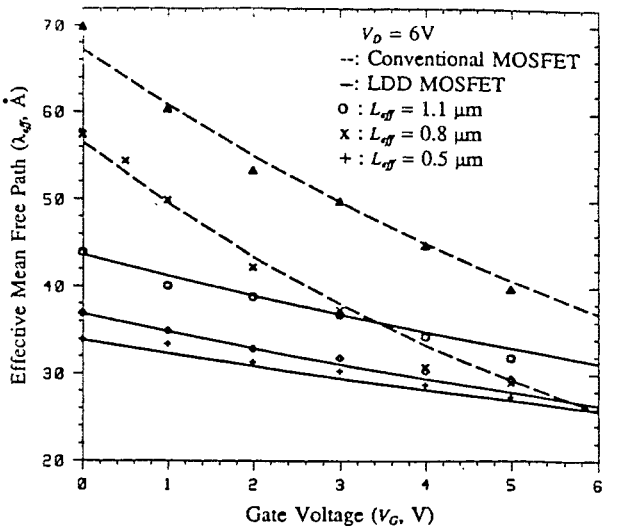


Fig. 4: Effective mean free path versus $V_G$ for conventional & LDD MOSFET devices. The solid & dotted lines represent model and points are the empirical data from experiment for $V_D$=6V

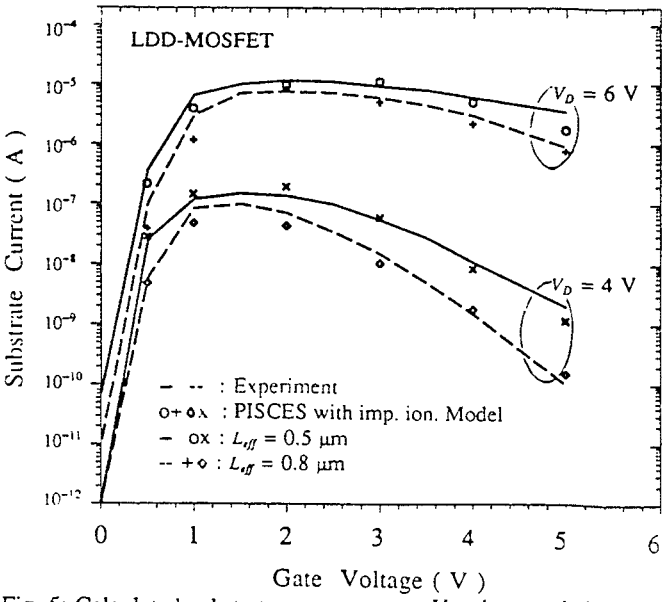


Fig. 5: Calculated substrate current versus $V_G$ characteristics. The results are for LDD MOSFET with 0.5 & 0.8 μm channel length.

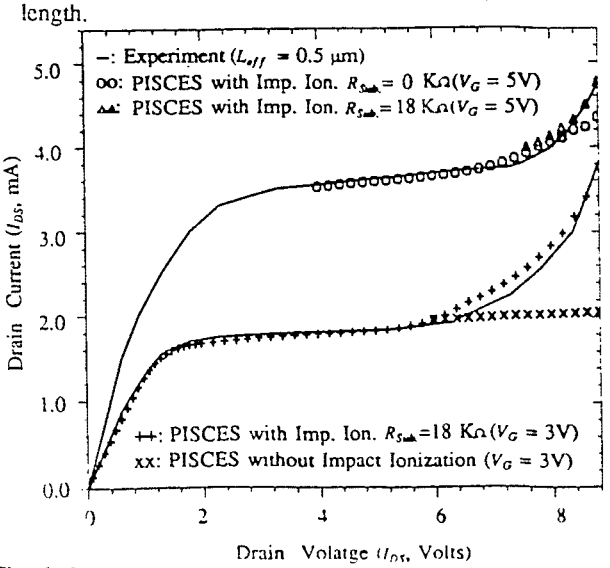


Fig. 6: Drain current versus drain voltage characteristics based on new impact ionization and modified mobility model