Impact of metal grain granularity on three gate-all-around advanced architectures

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***Abstract*—The impact of metal grain granularity (MGG) on the threshold voltage (V_{Th}) is compared for three different CMOS nanoscale multi-gate architectures with similar dimensions. The MGG of the gate stack induces the most pronounced variability in the device characteristics of non-planar architectures. We use the fluctuation sensitivity map (FSM) technique to evaluate which part of the channel beneath the gate is more affected by the MGG variability, and carry out a statistical study of the correlation between V_{Th} and the effective mean work-function (WF) of the gate. The nanosheet (NS) FET turns to be the most resilient architecture to the MGG with a threshold voltage standard deviation (σV_{Th}) of 104% and 54% lower than those of the nanowire (NW) FET and the FinFET, respectively.**

I. Introduction

THE continuous scaling of devices results in the increase of variability on their performance [1]. The metal grain granularity (MGG) is one of the most problematic sources of variability affecting the performance of different metal-oxide-semiconductor (MOS) devices [2]. A statistical comparison of the impact of MGG in different architectures can provide guidance for designing future MGG-resistant transistors. To achieve more resistant devices, the areas of the gate which are more impacted by the MGG might be identified to avoid the work-function variation effects on the metal deposition process [3].

In this work, we compare the influence of the MGG variability of different grain sizes (GS) on the threshold voltage (V_{Th}) for three state-of-the-art architectures: fin field-effect transistor (FinFET), gate-all-around (GAA) nanowire FET (NWFET) and GAA nanosheet FET (NSFET). The fluctuation sensitivity map (FSM) technique [4] is used to identify which zones of the metal gate are the most sensitive to the MGG for each architecture. Finally, the correlation between the V_{Th} and the mean work-function (WF) of the gate is discussed.

The structure of this paper is organised as follows: Section II includes the description of the devices, the simulation methodology used and the MGG implementation. Section III discusses the numerical results and Section IV summarises the main conclusions of this paper.

II. Device structure and simulation methodology

The benchmark devices are presented in Fig. 1 with their dimensions and doping values included in Table I. The FinFET and the NWFET dimensions and doping are scaled down from experimental transistors [5], [6], and the NSFET has the dimensions and doping of a experimental device [7]. We use VENDES [8], an in-house-built multi-method 3D finite element (FE) software simulation toolbox, that implements the drift-diffusion (DD) transport method while applying quantum corrections through the density gradient model (DG) for accuracy. I_D-V_G characteristics of all the three architectures were validated either against 3D FE quantum corrected (2D Schrödiger Eq.) Monte Carlo technique (also in VENDES [8]) [9], [10] or against experimental data when available [11].

The MGG variability is due to the random orientations of the metal grains produced in the gate deposition process [3]. Each grain orientation has a

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Table I
DEVICE DIMENSIONS FOR EACH ARCHITECTURE: GATE LENGTH L_G, SOURCE/DRAIN LENGTH $L_{S/D}$, CHANNEL WIDTH W, CHANNEL HEIGHT H, EFFECTIVE OXIDE THICKNESS EOT, GATE PERIMETER ρ_G, AND GATE AREA A_G. THE DEVICES HAVE AN UNIFORM p-TYPE DOPING (N_{ch}) IN THE CHANNEL AND A n-TYPE GAUSSIAN DOPING IN THE S/D REGIONS ($N_{S/D}$).

	FinFET	NWFET	NSFET
L_G [nm]	10.7	10	12
L_{SD} [nm]	10.7	14	14
W[nm]	5.8	5.7	50.0
H[nm]	15.0	7.2	5.0
EOT[nm]	0.62	0.8	1.0
ρ_G [nm]	35.8	20.3	110.0
A_G[nm^2]	383	203	1320
$N_{S/D}$ [cm^{-3}]	$1{\cdot}10^{20}$	$5{\cdot}10^{19}$	$5{\cdot}10^{19}$
N_{ch} [cm^{-3}]	$1{\cdot}10^{15}$	$1{\cdot}10^{15}$	$1{\cdot}10^{15}$

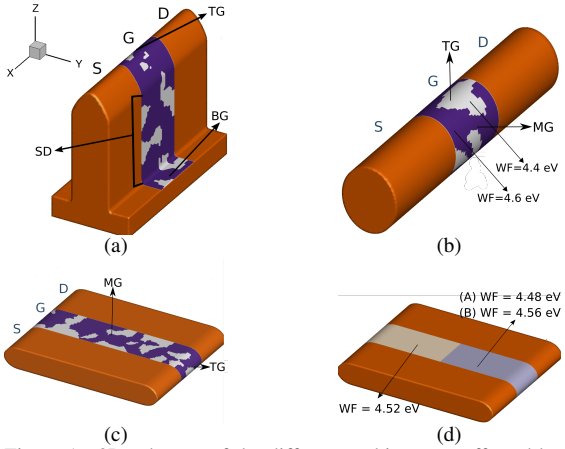

Figure 1. 3D schemes of the different architectures affected by arbitrary MGG (metal grain granularity) profiles. Realistic metal gate configurations are shown for (a) the 10.7 nm gate length FinFET, showing the sidewalls of the gate (SD), the top of the gate (TG), and the bottom of the gate (BG), (b) the 10 nm gate length NWFET, and (c) the 12 nm gate length NSFET. (d) A scheme of the 12 nm gate length NSFET affected with a synthetic MGG profile, showing the two hypothetical cases (A), and (B).

specific atomic surface density and therefore different values of WF [12]. The devices benchmarked in this work have a TiN metal gate which has two possible grain orientations: <200>/<111> with a WF of 4.6 eV/4.4 eV in occurrence probabilities of 60%/40% [12], respectively. The grains are constructed using Poisson-Voronoi diagrams [13] which reproduce the physical structure of the grain patterns depending on the average grain size (GS) (see examples of the grain random distribution on Fig. 1a-1c). The simulation study is carried out at a 0.7 V drain bias. To extract the V_{Th}, the constant current criteria is chosen at a drain current of 2.0 μA/μm. We have generated an ensemble of 300 devices with random MGG configurations for each architecture and GS, to make the statistical study.

III. MGG VARIABILITY COMPARISON

The MGG induced V_{Th} variability in the three state-of-the-art architectures is reported here. Fig. 2 shows the V_{Th} distributions for the NSFET (a), the NWFET (b), and the FinFET (c). Fig. 2 presents the mean V_{Th} of the distribution $\overline{V_{Th}}$ (blue line), the idealistic $V_{Th,ideal}$ (red line) of the device with a uniform gate (WF=4.52 eV), and the V_{Th} standard deviation σV_{Th}, which increases with the GS. The comparison between the σV$_{Th}$ for the three architectures at a GS of 7 nm shows that the NWFET is a 33%, and 104% more affected than the FinFET, and NSFET, respectively. The NSFET is the least affected architecture because the larger the gate area (A_G) the lower the expected effect on the conduction channel (see A_G values in Table I).

We define the threshold voltage shift ΔV_{Th} as the difference between $\overline{V_{Th}}$ and $V_{th,ideal}$. The distributions for the NSFET in Fig. 2a show a negative ΔV_{Th} that increases with the GS from -3 mV at GS=3 nm to -11 mV at GS=10 nm. For the NWFET in Fig. 2b, we can see a smaller increase of ΔV_{Th} than in the NSFET, from -1 mV at GS=3 nm to -5 mV at GS=7 nm. In the NWFET, the V_{Th} distribution for GS=10 nm do not follow the shift tendency because there are only a few grains in the gate with extreme WF values approaching the $\overline{V_{Th}}$ to $V_{th,ideal}$. Figs. 2a-2b show a negative shift ($\Delta V_{Th} < 0$) to smaller values. This shift is opposite to the expected with the increase of GS, because at a larger GS, the most probable WF value (60%, 4.6 eV) will dominate (the higher WF implies a higher V$_{Th}$), inducing a positive shift ($\Delta V_{Th} > 0$) to larger values in the V$_{Th}$ distributions. To understand this behaviour, we have created two synthetic MGG profiles (identified as A and B) in which the gate is divided into two identical zones with two different WFs, as shown in Fig. 1d. One zone has the

WF of 4.52 eV and the other of (A)4.48 eV/(B)4.56 eV. We define $\Delta V_{Th,low}$=$V_{Th,A} - V_{Th,ideal}$, and $\Delta V_{th,high}$=$V_{Th,B} - V_{Th,ideal}$, as the difference in V_{Th} between the ideal and the synthetic profiles with a low and a high WF. The influence of the low WF grains $\Delta V_{Th,low}$=-25 mV is larger for the NSFET than the influence of the high WF grains, giving $\Delta V_{th,high}$=16 mV. For the FinFET (-18 mV, 16 mV) and the NWFET (-21 mV, 19 mV), the difference is not so large but we see the same effect $|\Delta V_{Th,low}| > |\Delta V_{Th,high}|$. Hence, the grains with the low WF affect the V_{Th} more, producing percolation paths whereby the current can pass, lowering the potential needed to switch on the transistor. Note that the observed $|\Delta V_{Th}|$ is higher in the NSFET than in the other architectures because the current has a larger effective area of the channel to find percolation paths to flow.

Fig. 3 displays the V_{Th} FSMs for each architecture due to the MGG with GS=5 nm. Since the 3D gates have been resized to 2D planes, we indicate the different parts of the gate as follow: TG/MG/BG are the top/middle/bottom of the gate, SD are the sidewall of the gate, and SG/DG the source/drain gate interface (see their 3D location on Fig. 1). Fig. 3a illustrates that the most sensitive gate zones in the NSFET are the ones located on the MG and the center of the conduction channel. The TG zones are only slightly affected by the MGG (see Fig. 1c). The FSM of the NWFET (Fig. 3b) shows that the most sensitivity zones are the TG/SG regions and the center of the channel in the MG, all being less influenced by the grains located near the DG interface (see Fig. 1b). Fig. 3c shows the grains located on the SD in the FinFETs (see Fig. 1c). The grains located on the center of the gate have the most impact over the conduction channel, being the SD the most sensitive zones.

Fig. 4 shows the scatter plot between V_{Th} and the mean WF for each of the MGG profile. The Pearson's correlation coefficient CC is also shown. Note that, the NSFET $CC = 0.886$ and the NWFET $CC = 0.972$ in Fig. 4a-4b, display a high correlation between V_{Th} and WF. However, the FinFET (Fig. 4c) has no correlation ($CC = 0.409$) between V_{Th} and WF. The absence of correlation is due

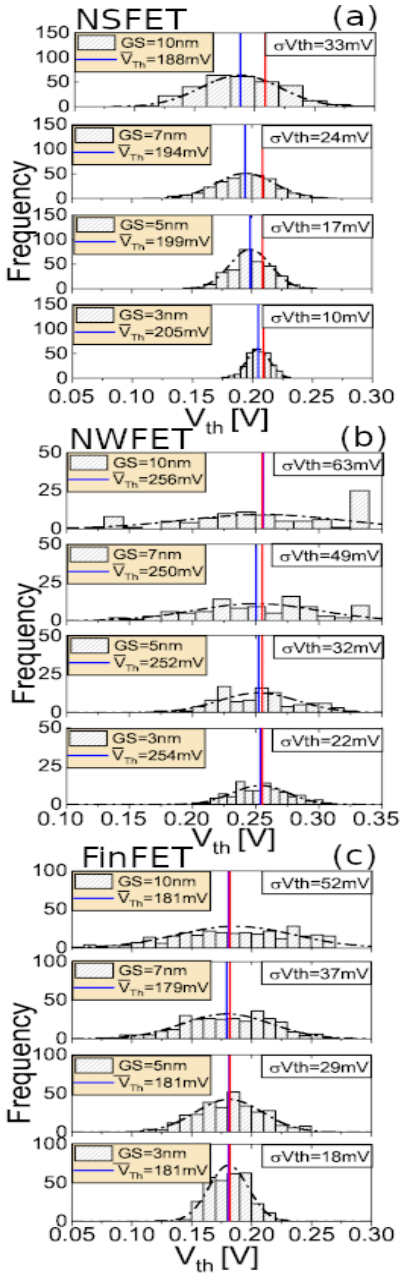

Figure 2. Threshold voltage (V_{Th}) histograms due to the MGG for different grain sizes (GS) for (a) the 12 nm gate length NSFET, (b) the 10 nm gate length NWFET, and (c) the 10.7 nm gate length FinFET. σV_{th} is the threshold voltage standard deviation, $\overline{V_{Th}}$ the mean values of the distributions (blue line), and $V_{Th,ideal}$ the idealistic value (red line) of the device with a uniform gate (WF=4.52 eV): 209 mV for NSFET, 255 mV for NWFET, and 182 mV for FinFET.

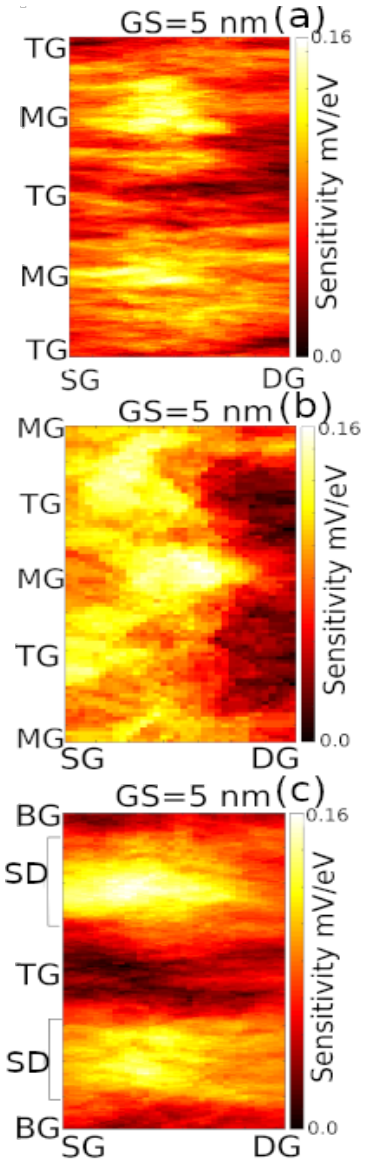

Figure 3. FSM of the V_{Th} at a GS 5 nm of (a) the 12 nm gate length NSFET, (b) the 10 nm gate length NWFET, and (c) the 10.7 nm gate length FinFET, where SG/DG are the source/drain gate interfaces, TG/MG/BG are top/middle/bottom of the gate and SD are the sidewalls of the gate.

to the grains located on the TG, and on the BG, which do not contribute to the gate control over the channel as shown in Fig. 3c, that could be responsible for the absence of the increase of ΔV_{Th} with the GS on Fig. 2c. Therefore, we repeat the

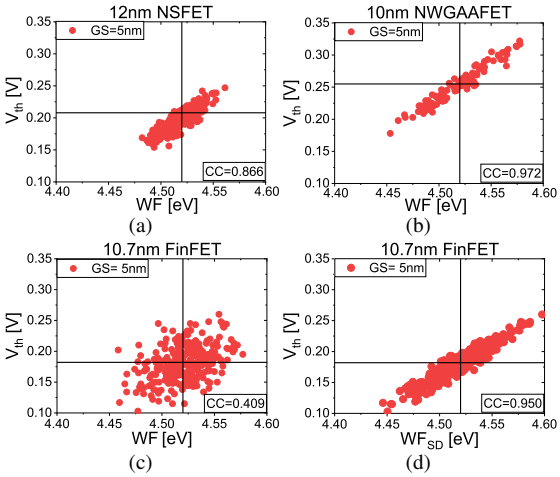

Figure 4. Scatter plot between the V_{Th} and the mean WF of the gate for each MGG profile at a GS=5 nm for (a) the 12 nm NSFET, (b) the 10 nm NWFET, (c) the 10.7 nm FinFET, and (d) the 10.7 nm FinFET with the mean WF of SD grains (WF_{SD}). The black lines represent the continuous WF of 4.52 eV and his associated $V_{Th,ideal}$. CC is the Pearson's correlation coefficient.

scatter plot taking into account only the mean WF of grains on the sidewalls (WF_{SD}), as shown in Fig. 4d with a $CC = 0.950$.

IV. Conclusions

We analyse the MGG induced variability on V_{Th} for the three architectures. The NSFET is the less affected with a σV_{Th} 104% and 54% smaller than the NWFET and the FinFET, respectively.

A negative shift to smaller values is observed in the mean V_{Th} of the distribution ($\overline{V_{Th}}$) from the ideal $V_{Th,ideal}$ due to the increase of the grain size (GS). This effect occurs because the lower WF grains have a greater influence on the V_{Th} distribution, producing percolation paths whereby the current can flow, lowering the potential needed to switch on the transistor. The grains sited on the top and bottom of the gate (TG/BG) of the FinFETs have no influence on variability, resulting in a lack of correlation between the V_{Th} and the mean WF of the gate. These results could have implications on the development of MGG-resistant metal gate configurations for advanced semiconductor devices.

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