Analysis of Thermal Concentration Failure in Unclamped Inductive Switching Based on Three-Dimensional Electro-Thermal Simulation With On-Chip Variation

Kyohei Shimozato, Yohei Nakamura and Takashi Sato
Graduate School of Informatics, Kyoto University,
Yoshida-hon-machi, Sakyo, Kyoto 606-8501, Japan
paper@easter.kuee.kyoto-u.ac.jp

***Abstract*—The analysis of failure development in unclamped inductive switching (UIS) is one of the most important aspects for improving the robustness of power MOSFETs. The observation of the failed chip surface revealed that the UIS failure occurs in a small area. No conventional simulation method has successfully reproduced this confinement because spatial variation of current and temperature on the chips have been ignored. In this study, we propose a three dimensional electro-thermal simulation method for UIS failure analysis. Our simulation result has shown significant current concentration due to the positive interdependence between local temperature and drain current in the intrinsic operation. In our simulation, the temperature of the failure region reaches over 4600 K.**

I. Introduction

SiC MOSFETs are promising switching devices for designing high power converters. SiC MOSFETs provide excellent specifications, such as low on-resistance, high withstand voltage in off-state, high temperature operation, and high frequency switching owing to the outstanding characteristics of SiC material as power devices. For example, the band gap is three times wider compared to the conventional Si material and thermal conductivity is as large as copper [1].

As SiC MOSFETs are used in crucial applications that support social infrastructures, such as railroad and automobile industries, their reliability is extremely important. A vast amount of studies have been carried out on unclamped inductive switching (UIS) because it is one of the most important failure mechanisms [2]–[7]. UIS test is a switching test with a circuit consisting of a MOSFET and an inductor connected in series (Fig. 1). When the MOSFET turns off, a high voltage is applied to the MOSFET, causing an avalanche current to flow until the energy stored in the inductor is consumed. If that energy is too large, short-circuit failure of the MOSFET occurs.

Despite these studies, there still exists a lot of debate about the cause of UIS, as summarized in Table I. Several different factors are considered as its dominant cause, which include

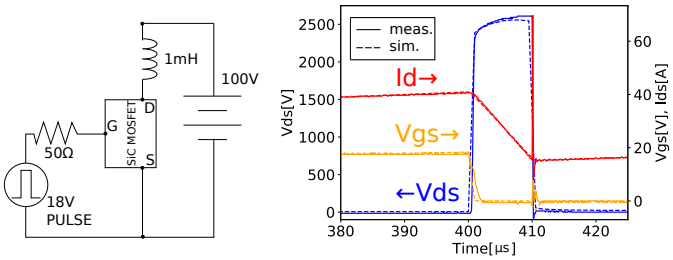

Fig. 1: UIS test circuit and its waveforms.

parasitic BJT operation [3], [5], intrinsic operation of SiC substrate [8], and the fusion of Al electrode [2].

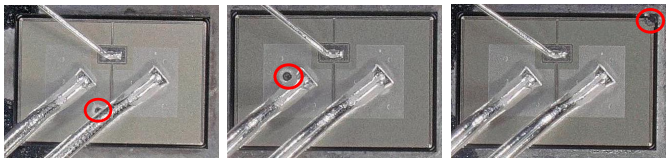

Fig. 2: Failure locations (circled) caused by UIS.

Fig. 2 shows the photographs of the chip surface on which the UIS failure has been observed. Though the locations of the failure vary in these three devices, the failures themselves are always concentrated in a small area, while the other die areas appear unaffected. As a result of cross-sectional observation, [7] reported that after the UIS failure, a hole was made through the substrate from top to bottom. However, in Table I, the critical temperature is considered at around 600°C. Given the melting point of SiC, the reported temperatures look too low to produce such a hole.

In order to analyze such local failure phenomena, it is necessary to consider three dimensional variation of current and temperature in a chip. However, as shown in Table I, no conventional simulation methods have considered the spatial variation. We hence propose a new three-dimensional electro-thermal (3D-ET) simulation method to investigate a failure mechanism of the UIS. The contribution of the proposed method is as follows:

978-1-6654-0685-7/21/$31.00 ©2021 IEEE

TABLE I: Comparison of simulation methods for analyzing failure mechanism of UIS.

Ref.	Analysis method	Target scale	Cause of failure	Critical temp.	Variation
[2]	TCAD sim.	About 10 cells	Fusion of Al electrode	660°C	Only in 2D
[3]	TCAD sim.	Single cell	Parasitic BJT	-	No
[5]	TCAD sim. / Numerical analysis	Single cell / Whole die	Parasitic BJT	600°C	No
[6]	SPICE sim.	Whole die	-	-	No
[7]	Numerical analysis	Whole die	Chemical reaction	650°C	No
[4]	SEM image	Broken point	Micro-pipe defects	-	-
This work	3D-ET SPICE sim.	Whole die	Intrinsic operation	4600K	Yes

- On-chip spatial variation of current and temperature is considered.
- Potential failure mechanisms are modeled as an equivalent circuit considering temperature dependence.
- A full chip analysis is made possible through SPICE-based modeling and simulation.

II. 3D-ET Simulation Methodology

The overview of the proposed circuit model for the 3D-ET simulation is shown in Fig. 3. According to the physical layout, a MOSFET is divided into sections, each consisting of an electrical and a thermal circuit in order to analyze the on-die current and temperature variations simultaneously. The size of the section corresponds to a few elementary cells of the MOSFET. Each section is further divided into layers. In this example consists of five layers in total, with a channel region layer and four layers of the drift region.

In addition to the basic elements [9], such as channel, parasitic capacitances, drift resistance, each section includes two avalanche-related components [8], (a) parasitic BJT and body diode (BD) at NPN junction, (b) intrinsic resistance (R_{id}) that represents decreasing resistance of SiC substrate at high temperature. P_0 to P_4 in the thermal circuit represents the heat generation of each layer which is calculated by the electrical counterpart. The temperature of each layer, T_0 to T_4 are referenced by the elements in the corresponding layer of the electronic circuit. The red dots in a section represents the crosspoint of the meshes. The adjacent sections are connected three-dimensionally via specific resistances.

The current characteristic of the channel, the drift resistances, the parasitic capacitance, and the breakdown voltage of the body diode are modeled based on the parameter extraction from the measurements, while the other elements are defined according to the material properties [10]. All elements in the electronic and thermal circuits, except the parasitic capacitance, possess a temperature dependence [8], [9]. Note that the thermal resistance increases rapidly, indicating that the heat would not spread rapdly in a higher temperature range.

III. Experimental Validation and Discussion

In this section, a commercial SiC MOSFET, ROHM SCT2080KE, is analyzed. Each section represents 5x5 elementary cells. The thickness of the channel layer is 2 μm and that of each drift layer is 5 μm. The random component of the spatial breakdown voltage variation of the body diode is considered as a zero-mean normal distribution with a standard deviation of 30 V [11], [12] (Fig. 4). The breakdown voltage of the body diode of the i-th section is defined as:

$$V_{\mathrm{BD},i} = V_{\mathrm{BD,device}}(T) + \Delta V_{\mathrm{BD},i}. \tag{1}$$

$V_{\mathrm{BD,device}}(T)$ is the breakdown voltage of a device with linear temperature dependence, whose coefficients are derived experimentally. $V_{\mathrm{BD,device}}$ at 25°C is 2380 V. The variation $\Delta V_{\mathrm{BD},i}$ generated as a sample from a zero-mean 30 V standard variation is considered sufficiently small. Most of the samples are within ±5% of the nominal value. The components in our model are implemented using Verilog-A as an equivalent circuit. The simulation requires about 100 minutes for a single run.

Fig. 1 shows the simulation and measured waveforms. The simulation reproduced the overall device operation very well. Fig. 5 shows the development of the current density I_{ch} and temperature T_{j} of the channel layer. At 401 μs, immediately after the avalanche event started, the temperature increases rapidly. Then, at 410 μs, the current concentrates in one section, increasing the temperature of the section to 4619K which leads to the failure. Since the melting point of SiC is about 2730 K and that of aluminum is about 900 K, MOSFETs will deform in the highest temperature area and fail electrically.

Referring to Fig. 4, the failure section has the smallest breakdown voltage among all. When a failure occurs, the failure area spreads to neighboring sections in a short time, while the temperature of other sections drops quickly. This phenomenon is caused by the temperature dependence of the thermal circuits, i.e., the heat flow to the surrounding sections or layers is reduced at high temperature. This operation agrees very well with pinhole-like failures observed in Fig. 2. Furthermore, the size of the failure region agrees well (Fig. 6).

In terms of three-dimensional variation, Fig. 7 shows the distribution of temperature and current density on each layer. From this result, we see that the failure point is very localized. The current does not spread to other areas even in the drain-side layers. Moreover, according to the simulation result, no current flows through the BJTs, indicating the dominant cause of the failure is the intrinsic operation of SiC material. The temperature gradient in the drain-source direction is also remarkable. T_{j} of most sections is about 1000 K at 410 μs, while T_4 remains about the ambient temperature even after the failure occurred. This result suggests that three-dimensional variation of temperature and current is not ignorable in order to analyze the UIS. Though it is difficult to measure the on-chip variation of the real chip, even a slight variation of the breakdown voltage can cause the pinhole-like failures.

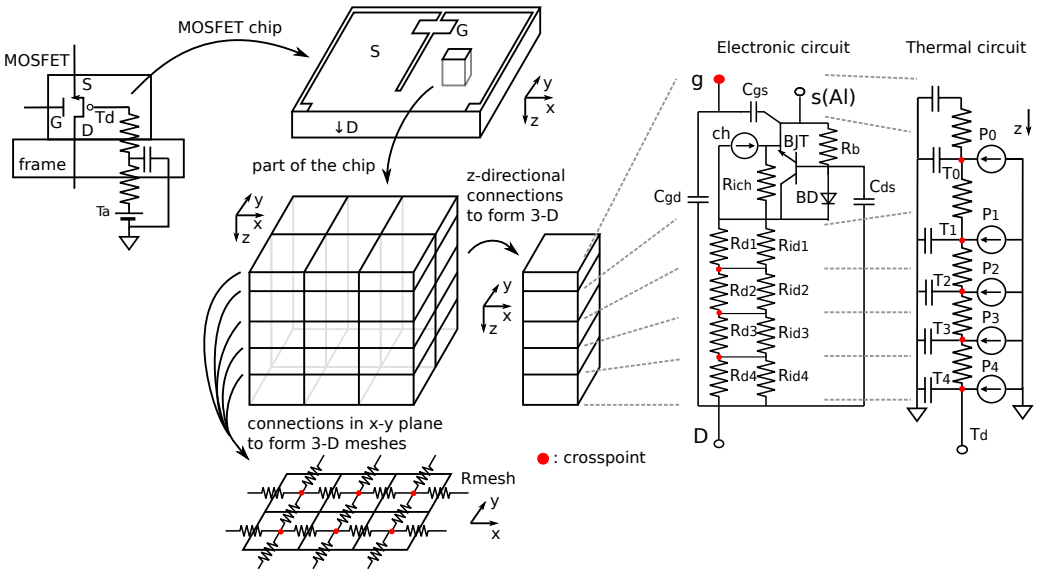

Fig. 3: Overall structure of the 3D-ET equivalent circuit for the proposed analyses.

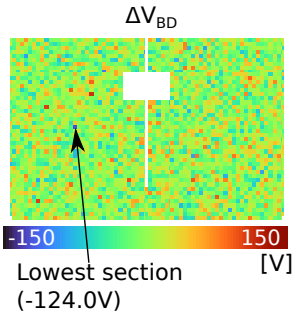

Fig. 4: Simulated breakdown voltage variation on a chip. The color scale shows the difference from the mean breakdown voltage.

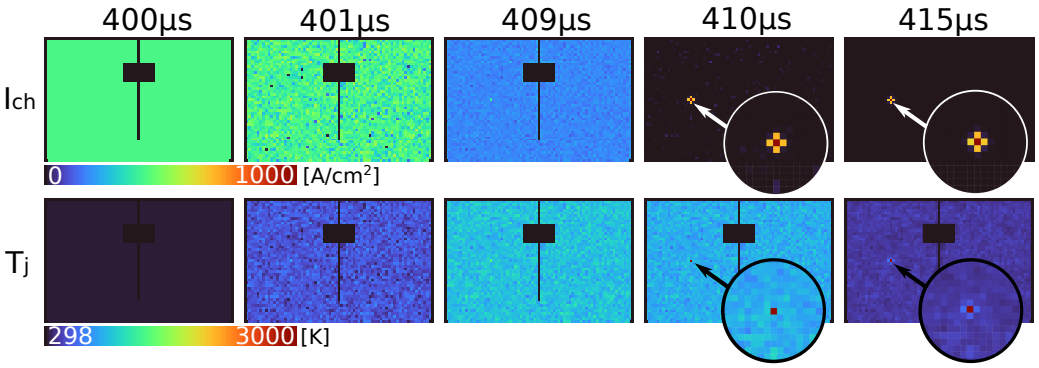

Fig. 5: Transient change of current density I_{ch} and temperature T_j in the channel layer. I_{ch} and T_j reaches 418191 A/cm^2 and 4619 K, respectively, at 410 μs. Once the current starts to concentrate, the current of other sections decreases quickly. Temperature change also follows a similar trend but with a slight delay.

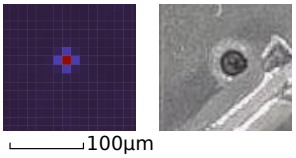

Fig. 6: Simulated junction temperature around the failure point at 425 μs and the failure point of a chip after UIS failure at the same scale.

As shown in Figs. 4 and 5, the failure occurs in the section with the lowest breakdown voltage. This section is most likely to be the first on the chip to experience an avalanche. Thus the temperature will be highest in the early stages of the avalanche event. However, the drift resistance of that section also increases, resulting that the current flowing through it would be smaller than the other sections after the avalanche event spreads over the whole die.

According to the waveforms of I_{ch} and T_j of all sections during the avalanche event (Fig. 8), the current of the weakest section once decreases during the avalanche event. Currents of other sections can become higher. However, T_j of the weakest section is always higher than the other sections throughout the avalanche event. Fig. 9 shows the correlation between ΔV_{BD}, I_{ch} and T_j at 409 μs, just before the failure. I_{ch} correlates with ΔV_{BD} for the majority of sections, except for a few sections. This is understandable because higher current flows through the sections near the source electrodes, and vice versa. Meanwhile, T_j correlates with ΔV_{BD} perfectly. From these results, the failure occurs at the weakest section, even though I_{ch} can be less than other sections during the avalanche event.

In the above simulations, we assumed the variation of breakdown voltage follows a normal distribution with a standard deviation of 30 V. The correlation between the standard deviation and UIS tolerance is studied. As shown in Fig. 10, the larger the variation the worse the tolerance of UIS. The transition between the fail and pass conditions is gradual, which can be explained by the difference in the weakest sections and their position in a chip.

IV. Conclusion

We conclude that the model representing the 3D variation of both temperature and current is critical in order to analyze the UIS failure. The failure is likely to occur in the section with lowest ΔV_{BD}. The construct of the proposed simulation model is applicable for any power devices.

ACKOWLEDGEMENT

This work was supported by JST-OPERA Program Grant Number JPMJOP1841, Japan.

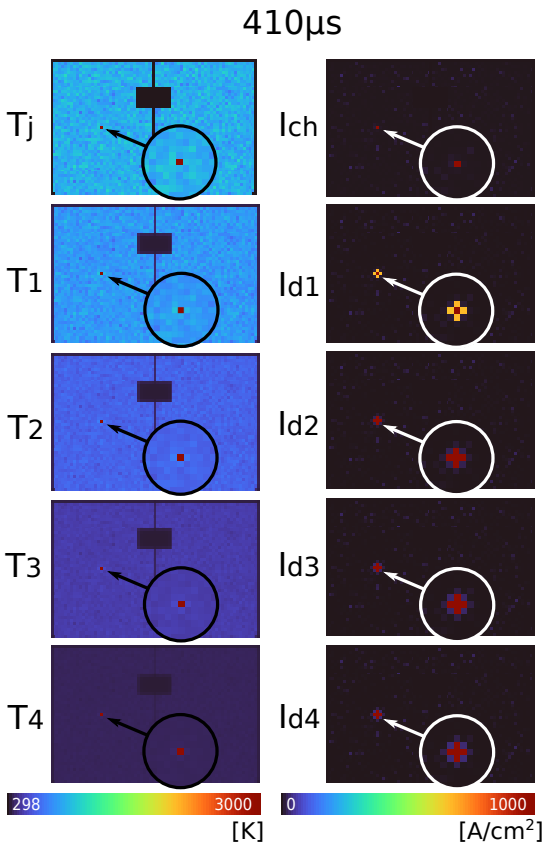

Fig. 7: Temperature and current of each layer after the failure.

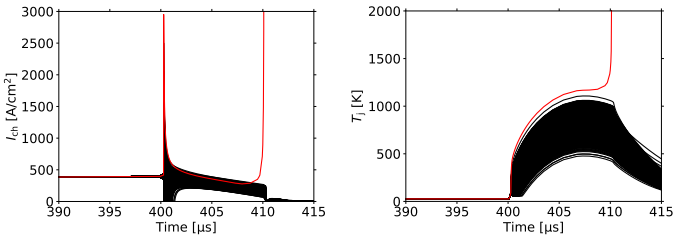

Fig. 8: Transient waveform of I_{ch} and T_j of all sections. Red lines indicate that of the section with the lowest ΔV_{BD}.

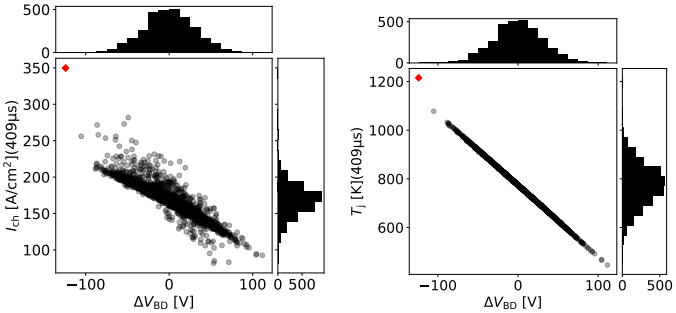

Fig. 9: Correlation between ΔV_{BD}, I_{ch}, and T_j of sections at 409 μs. Diamond symbol indicates the section with the lowest ΔV_{BD}.

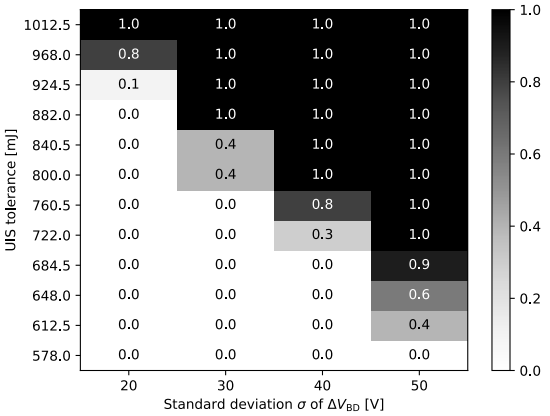

Fig. 10: Failure rate of different Standard deviation of ΔV_{BD} and UIS tolerance. UIS tolerance is defined by the energy stored in the inductor before the UIS.

References

[1] T. Kimoto and J. A. Cooper, *Fundamentals of silicon carbide technology: growth, characterization, devices and applications*. US: John Wiley & Sons, 2014.

[2] S. Liu, X. Tong, J. Wei, and W. Sun, "Single-pulse avalanche failure investigations of Si-SJ-MOSFET and SiC-MOSFET by step-control infrared thermography method," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 5180–5189, May 2020.

[3] A. F. Witulski, D. R. Ball, K. F. Galloway, A. Javanainen, J.-M. Lauenstein, A. L. Sternberg, and R. D. Schrimpf, "Single-event burnout mechanisms in SiC power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1951–1955, Aug. 2018.

[4] K. Hasegawa, K. Taguchi, Y. Kagawa, E. Suekawa, N. Kaguchi, Y. Ata, H. Haruguchi, Y. Nakashima, and T. Minato, "Which is harder SOA test for SiC MOSFET to do Unclamped Inductive Switching (UIS) or Unloaded Short Circuit mode Switching (USCS)? Does UIS play a role of USCS?" in *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 62–65.

[5] N. Ren, H. Hu, X. Lyu, J. Wu, H. Xu, R. Li, Z. Zuo, K. Wang, and K. Sheng, "Investigation on single pulse avalanche failure of SiC MOSFET and Si IGBT," *Solid-State Electronics*, vol. 152, pp. 33–40, Feb. 2019.

[6] M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio, and A. Irace, "A temperature-dependent SPICE model of SiC power MOSFETs for within and out-of-SOA simulations," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8020–8029, Sep. 2018.

[7] A. Konstantinov, F. Allerstam, H. Pham, G. Park, K. S. Park, D. Waible, and T. Neyer, "Critical temperature and failure mechanism of SiC schottky rectifiers in Unclamped Inductive Switching (UIS)," in *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 158–161.

[8] K. Shimozato, Y. Nakamura, S. Bian, and T. Sato, "An electrothermal compact model of SiC MOSFETs for analyzing avalanche failure mechanisms," *Japanese Journal of Applied Physics*, vol. 60, p. SBBD11, Feb. 2021.

[9] K. Shimozato, S. Bian, and T. Sato, "A compact device model for SiC MOSFETs valid for wide-temperature range," in *IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA-Asia)*, Sep. 2020, pp. 56–60.

[10] A. Tsibizov, I. Kovačević-Badstübner, B. Kakarla, and U. Grossner, "Accurate temperature estimation of SiC power mosfets under extreme operating conditions," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1855–1865, Feb. 2020.

[11] Y. Cui, X. Hu, X. Xie, R. Wang, and X. Xu, "Spatial variation of lattice plane bending of 4H-SiC substrates," *CrystEngComm*, vol. 19, no. 27, pp. 3844–3849, 2017.

[12] N. A. Mahadik, H. Das, S. Stoupin, R. E. Stahlbush, P. L. Bonanno, X. Xu, V. Rengarajan, and G. E. Ruland, "Evolution of lattice distortions in 4H-SiC wafers with varying doping," *Scientific Reports*, vol. 10, no. 1, p. 10845, Jul. 2020.