Materials and Device Strategies for Nanoelectronic 3D Heterogeneous Integration

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***Abstract*—Monolithic 3D heterogeneous integration is the most cost effective route to realize continued scaling in power and performance in integrated circuit technologies. In this paper, we discuss a variety of methods, materials, and device concepts to help overcome the constraints imposed by putting active devices in the upper levels. Our focus is on realizing better materials at low processing temperature for logic, memory, and dense interconnects taking advantage of unique physics to surmount current limitations in 3D integrated device performance.**

Keywords—3D integration, low-temperature synthesis, 2D materials, topological materials, interconnects

I. Introduction

Greater than 60% of compute performance gain over the past decade can be attributed to innovations in semiconductors including 40% due to process technology improvements like denser, high-performance transistors and RC reduction in the back-end [1]. The introduction of new materials and device structures has enabled the industry to maintain scaling trends, trends that continue to this day. However, to realize even further gains in power, performance, and density scaling, a move to 3D integration is going to be necessary. Monolithic 3D integration, with logic and memory co-located in the upper levels above the high-performance compute devices coupled with dense, nanoscale interconnects, could offer massive systems-level energy-delay-product gains [2].

However, there are immense challenges associated with making high-quality materials and devices in these upper levels without damaging the underlying layers. In particular, the severe constraint on thermal budget (all processing must remain below 450 °C) makes the synthesis of materials and devices that can support reasonable transport properties very difficult. Additional challenges with 3D integration include deposition on non-ideal surfaces, non-planar geometries, selectivity, and scalability, all of which lead to defects and degraded transport. In this paper, we discuss various ways of synthesizing high-quality materials for logic, memory, and interconnects that are compatible with back-end-of-line (BEOL) constraints.

II. Low-Temperature Growth of Semiconductors

A. Crystalline semiconductors

To achieve crystalline thin film growth, some percentage of the constituent elements must stick to the substrate after being evaporated, becoming adatoms. Those adatoms must migrate along the surface to either nucleate the next layer of the thin film or attach to an already existing nucleus. Each of these events is highly temperature dependent, needing to overcome kinetic barriers to achieve the higher quality equilibrium crystal structure. Only adatoms with sufficient energy can diffuse enough to reach the edge of the growth front and form 2D layer-by-layer growth. Typically, one simply increases the substrate temperature to provide the adatoms with enough energy to overcome those barriers. But BEOL compatible temperatures do not provide the adatoms with sufficient energy, resulting in 3D island growth. To enable higher-quality crystalline semiconductors grown at low temperatures, techniques have been developed to either reduce the energy barriers or by providing additional localized energy other than the substrate temperature to overcome the barriers.

B. Reducing kinetic energy barriers

Surfactants, extrinsic elements that reduce surface tension, are one way to reduce the diffusion energy barrier. Surfactant atoms usually have low solid solubility and a smaller bond energy with the host material, enabling easier surface migration and exchange with the constituent adatoms, overall enhancing layer-by-layer growth. Surfactants have been used in III-V and III-N growth for years and indium, arsenic, and bismuth have been demonstrated as effective surfactants in the growth of these materials. As an example of using surfactants to enable BEOL compatible crystal growth, our group has recently demonstrated that GaN grown at 450 °C, results in much higher quality crystal growth when Bi is used as a surfactant (Fig. 1a).

The vapor-liquid-solid (VLS) method of crystal growth is another method for lowering kinetic barriers associated with crystal growth, specifically for nanowires. A catalytic liquid droplet on a surface promotes the formation of a supersaturated liquid that lowers the active energy compared with the vapor-solid interface, enhancing the adsorption of vapor atoms onto the solid surface. The growth temperature is limited by the eutectic point of the mixture phase. Si nanowires have been grown with Au as the catalyst at 500 °C (the Au-Si eutectic point is 373 °C), a temperature much lower than the conventional growth temperature above 800 °C by CVD for example. The growth temperature can be further reduced to BEOL compatible temperatures by using other low melting temperature metals as the catalyst, like Ga [3]. VLS also benefits from being able to encode different functionalities, like doping or heterostructures by designing the gas phase mixture.

Migration enhanced epitaxy (MEE) is another method that enhances crystallinity at lower temperatures by lowering energy barriers. During the MEE process for compound semiconductor growth, the atomic sources are periodically

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interrupted, alternating which species impinges on the surface at a given time. By limiting the supply of one of the atoms, fewer nucleation events occur, and the diffusion energy barrier can be manipulated to enable longer adatom surface migration. In GaAs, for example, temperatures can be reduced by as much as 400 °C in some cases using MEE [4].

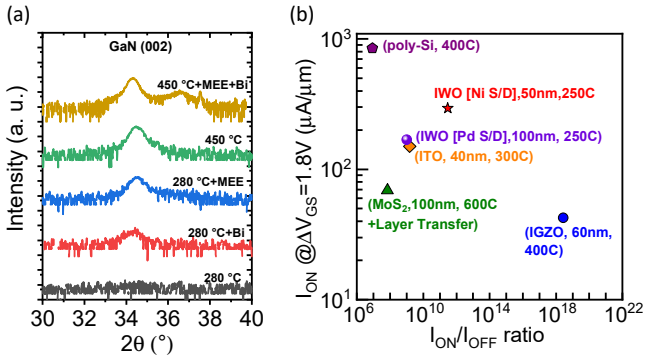

Fig.1 (a) X-ray diffraction data showing the enhancement of crystal quality of GaN grown at low temperatures when using MEE and Bi surfactants. (b) Benchmarked BEOL compatible thin-film transistor data showing amorphous oxides, 2D materials, and laser crystallized Si are all competitive. Reprinted with permission from [8].

C. *Supplying energy other than substrate temperature*

Rather than reducing the energy barrier, other crystalline growth strategies utilize the addition of extra energy to the thin film through means other than increasing the substrate temperature, protecting the other materials and devices. Plasma enhanced depositions are a good example of this by utilizing an additional energy source to pre-crack the gas precursor in MOCVD or ALD, which usually requires high-temperature thermal energy. In MOCVD GaN growth, one of the limiting factors, especially for low-temperature growth, is the decomposition of the N precursor. Remote plasma has been applied in pre-cracking NH_3 or N_2, in one case enabling reasonable electron mobilities at temperatures 300 °C lower than typical for GaN growth [5]. Plasma-enhanced ALD is also becoming a standard technique in semiconductor technologies.

Post-deposition anneals are another way of providing extra energy to reshape and improve crystalline materials. However, traditional techniques, such as rapid thermal annealing (RTA), expose the lower levels to unacceptably high temperatures. In contrast, laser annealing is gaining more traction for BEOL technologies due to the potential for very localized increased temperatures that can be designed to only impact the surface while the underlying devices are relatively unperturbed [6]. This method has been widely used in CMOS processing for dopant activation in junctions and is being utilized for crystallization of Si and Ge BEOL devices now.

D. *Entropy stabilization*

A unique way of obtaining new crystalline compounds is to use configurational entropy to stabilize multi-component materials into crystalline structures not typically observed. Usually composed of five or more constituent elements (so the entropy term wins out over the enthalpy penalty associated with adding additional components) the mixture transforms to a single-phase crystal when the temperature is high enough. For BEOL technologies where the thermal budget is limited, the temperature that allows the entropy to enable a random mixture can be provided through techniques such as pulsed laser deposition (PLD). The laser ablation of the multi-component source provides this energy at the source itself, and upon deposition at much lower substrate temperatures, this random mixture is quenched into its crystalline, entropy stabilized phase. This has been demonstrated in the (MgCoNiCuZn)O is system for a substrate temperature of 300 °C [7] as an example.

E. *Amorphous semiconductors*

Although crystalline semiconductors are preferred due to their better electrical transport and reliability, oftentimes at BEOL temperatures, they simply cannot be made. In those instances when amorphous materials are the likely result of growth conditions, it is important to strategically select which amorphous materials can support improved transport properties. Taking a page from the display industry, amorphous transition metal oxides like IGZO have an important role to play in 3D integration (Fig. 1b). Semiconductors like silicon have directional sp^3 orbitals, which support good transport when highly ordered (crystalline), but results in a severe mobility degradation when disordered (amorphous). In contrast, transition metal oxides, have spherically extended s orbitals, which enables mobilities that are much more robust to disorder resulting in satisfactory performance of amorphous materials deposited at low temperatures.

III. Layered Materials

A. *2D materials growth; relaxed lattice matching*

2D materials have garnered much interest over the past decade and longer due to their atomically thin structure, tunable bandgap, and unique optical, electronic, and spin properties. Transition metal dichalcogenides (TMDs) with the composition MX_2 (M = W or Mo, and X = S, Se, or Te), is a group of 2D materials in which the transition metal is covalently bonded to the chalcogens in a hexagonal structure within a layer. Monolayers are then stacked on top of one another through weak van der Waals forces. These materials are appealing for 3D integration as they can be grown epitaxially at relatively low temperatures on a variety of substrates with a significantly relaxed requirement on lattice matching. Various techniques including MBE, chemical vapor deposition (CVD), and even PLD have been demonstrated for large area growth. Our group demonstrated that TMDs can even be grown with preferred orientation on ALD grown amorphous oxides [9] at temperatures compatible with BEOL processing. These WSe_2 thin films were demonstrated to support room-temperature field effect hole mobilities up to 50 cm^2/V-s (Fig. 2b)

B. *Use as a growth template for 3D materials*

Recently, 2D materials have found special attention for improving the growth quality of traditional 3D semiconductors through a technique called remote epitaxy. Recent reports on the growth of nitrides and phosphides using a monolayer of graphene as an intermediate layer is very promising [10]. The ionic interaction between the substrate and the adatoms *through* the 2D intermediate layer, along with the atomically inert 2D surface, helps with the long-range diffusion of adatoms and improves the quality of the 3D material. Our research on the

growth of BEOL compatible GaN and ZnSe by using a monolayer of tungsten diselenide (WSe_2) as a template shows significant improvement in growth quality (Fig. 2c) and mobility enhancement. 2D materials have also been demonstrated as a good growth template for elemental metals, resulting in much larger grains. Utilizing 2D materials as a growth template for higher-quality, low-temperature grown 3D materials appears quite promising for BEOL applications.

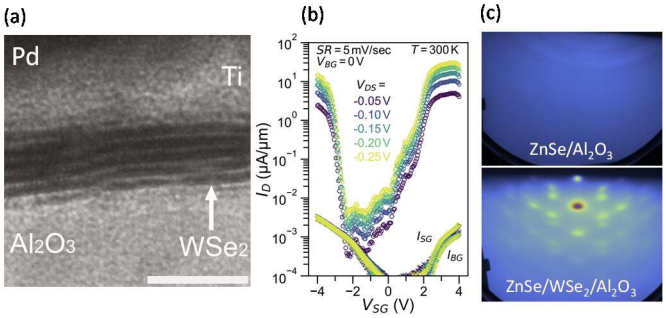

Fig.2 (a) TEM image of a 6 monolayer thick WSe_2 thin film grown on amorphous Al_2O_3 grown in the Hinkle lab. (b) Transfer characteristics of a transistor made from the structure in (a) with hole mobilities of ~50 cm^2/V-s. Preprinted with permission from [9]. (c) Improvement in growth quality of ZnSe achieved by using a 2D intermediate layer. RHEED pattern transitions from Debye rings to streaky dots confirming better quality of the film.

C. 2D materials for magnetic memory

Apart from the inclusion of 2D materials as an active layer for transistors, they are also being researched for magnetic memory applications following the observation of low temperature ferromagnetism in monolayers of CrI_3 and $Cr_2Ge_2Te_6$. Our group is working on magnetic impurity doped TMDs, which density functional theory (DFT) and Monte Carlo simulations have identified as having the potential to exhibit above room temperature magnetism [11]. Substitutional doping of 15% Fe in WSe_2, for example, is predicted to give a 2D ferromagnet with a *Curie* temperature of >320 K and in-plane magnetic anisotropy. Chromium doping in WSe_2, on the other hand, is predicted to have an antiferromagnetic ground state. These 2D magnets are ideal candidates for magneto-electric (ME) switching-based devices in which the 2D ferromagnet couples with the ME through exchange coupling, which is thickness dependent. Memory, as well as logic devices based on magnetoelectric switching, have been envisioned to consume <1 atto-joule (aJ) of energy which is orders of magnitude lower than state-of-the-art devices.

D. Topological Insulators

Many topologically protected materials are also layered materials, having the same relaxed criteria for lattice matching as the TMDs. Topological systems that have surface states that are spin-momentum locked so that point defects and line roughness have minimal effect on the carrier transport due to the suppression of backscattering are appealing in BEOL devices where defects are inevitable due to the low temperature processing. Novel device concepts are already in place including a proposed topological insulator field effect transistor [12], or integrating a topological insulator (e.g. Bi_2Se_3) or topological semimetal with ferromagnets for spin-orbit-torque and spin-transfer-torque based devices [13].

IV. Nanoscale Interconnects

A. New metals needed to replace Cu

The continued scaling of integrated circuits and the potential move to monolithic 3D integration requires high-performance nanoscale interconnects. State-of-the-art Cu interconnects have become a critical bottleneck at these dimensions, causing RC delays even exceeding gate delay from the front-end-of-line [14]. When the metal linewidth is smaller than the electron mean-free-path of Cu (~40 nm), the resistivity of Cu increases significantly with a decreasing cross-section due to increased surface and grain boundary scattering (Fig. 3). It is found that both of these scattering processes are proportional to the product of the bulk resistivity and the bulk mean free path $\rho_0\lambda$, which serves as a figure of merit for ultra-thin film resistivity size effects as developed by Gall [15]. Moreover, $\rho_0\lambda$ can be calculated solely based on the Fermi surface within the classical transport description. In this framework, it is found that some other elemental metals such as Ir and Rh have smaller $\rho_0\lambda$ than Cu. As seen in experimental measurements, their resistivities remain relatively unchanged as thickness decreases, and can be expected to compete with Cu at sub-10 nm thickness. Furthermore, the $\rho_0\lambda$ can be used as a metric to screen for new materials. Calculations have screened a group of layered ternary carbides and nitrides $M_{n+1}AX_n$ phase [16], e.g., Cr_2AlC and Ti_4SiC_3, showing much smaller in-plane $\rho_0\lambda$ than Cu, due to their anisotropic transport and smooth, layered structures reducing surface scattering. The MAX phases also show excellent mechanical and thermal properties, and are therefore under investigation as a replacement for Cu for BEOL interconnects.

B. 2D materials for barriers/liners

Another challenge with nanoscale interconnects is the need to include a Ta/TaN liner/barrier to prevent issues with electromigration of Cu. The high-resistivity Ta/TaN stack must be at least 3 nm in order to effectively prevent Cu diffusion into the surrounding low-k dielectrics [17] taking up an ever-increasing percentage of the interconnect volume, exacerbating resistivity scaling. 2D materials have been proposed as sub-nm ultra-thin barrier/liners enabling better scaling metrics. Experiments provided early evidence that single-layer graphene can prevent Cu diffusion comparable to 4 nm TaN tested by time-dependent dielectric breakdown (TDDB) [18]. However, the high temperature processing to synthesize graphene prevents challenges to its inclusion for liners in the BEOL. The aforementioned TMDs, in contrast, can be prepared at BEOL compatible temperatures (< 450 °C). A 1.5 nm TaS_2 thin film was demonstrated as a diffusion barrier with comparable performance compared to 2 nm TaN [19]. Moreover, despite weak van der Waals (vdW) bonds of the surface of 2D materials, excellent wetting and adhesion of TaS_2 to SiCOH-based low-k dielectrics has been demonstrated, assuring reliability against CMP processes in IC fabrication. Moreover, 2D materials (e.g., MoS_2, TaS_2) exhibit another characteristic in that Cu (and other metals) deposited on them has smaller resistivity compared to those grown on SiO_2. This is due to the improvement of specular surface scattering by using 2D materials in conjunction with the weak vdW bonds facilitating long-range diffusion of the metal adatoms, enabling

the formation of larger Cu grains. 2D materials could be a promising candidate to replace the current Ta/TaN liner/barrier.

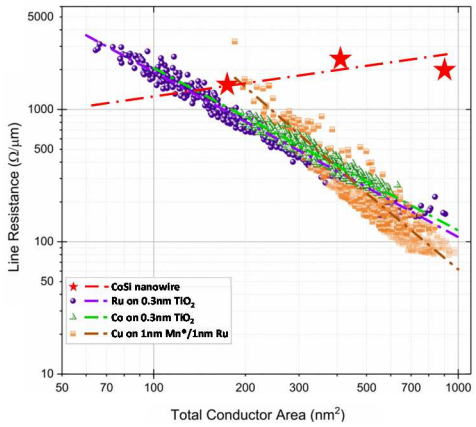

Fig. 3 Line resistance versus total conductor cross-sectional area of Ru, Co and Cu nanowires compared with CoSi nanowires. The topological states in CoSi enable the reduction in resistance with smaller dimensions, in contrast to conventional metals. Reprinted with permission from Crystal Growth & Design, 9, 4515 (2009) Copyright 2009 American Chemical Society. Reprinted with permission from 2018 IEEE IITC, pp. 172-174 Copyright 2018 IEEE.

C. Topological semimetals

Topological semimetals are an interesting option for scaled interconnects due to their unique properties. In contrast to conventional semimetals where the Fermi level crosses both the conduction and valence bands, the two bands of a topological semimetal touch at discrete nodes in *k*-space, leading to the formation of topology-protected, non-trivial surface states connecting nodes with opposite Chern numbers. The unique features of these surface states act to effectively suppress back-scattering. It has been experimentally demonstrated that the Weyl semimetal (2-fold band degeneracy at the nodes) NbAs shows significantly smaller resistivities when scaled down compared to their bulk values, even reaching as low as ~1 μΩ·cm [20], due to the scattering suppressing surface states dominating conduction at small dimensions. This is, of course, in contrast to conventional metals whose resistivities get worse at smaller dimensions.

The multi-fold Fermion semimetal (multiple-fold degeneracy at the nodes) CoSi (Fig. 3) is another interesting option that seems to have these beneficial scaling trends [21], while also being compatible with Si-CMOS technology. Calculations on CoSi show that even in the presence of surface defects, ~75% of the conduction is carried by topologically protected surface states in sub-10 nm thick films. Topological metals have the potential to truly revolutionize scaled interconnects which are a critical component to dense 3D integration.

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