First-principle Extraction of Surface Roughness in Si/Oxide Interfaces

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***Abstract*—A novel algorithm is introduced to extract the electrical roughness at the first principle level. The auto-correlation and root-mean-squared height of roughness spectrum are extracted for 3×3 nm² Si/SiO_2 samples. As an application, the impact of Ge-O bond on electrical roughness is demonstrated. The result concludes that electrical roughness of a given interface can be substantially larger than geometrical values.**

Keywords—Surface roughness, auto-correlation function, density functional theory, impurity.

I. Introduction

To secure the electrostatic control, the channel cross section of short devices has to be shrunken. Such a constraint inevitably increases the surface to bulk ratio in transport domain. As a result, surface phenomena grows to be essential for all scaled devices. From transport point of view, two noticeable sources of scattering are surface roughness and surface phonons [1]. The latter one regards the deviation of sound velocity and atomic vibration around the interface, while the former concerns the modulation of quantum well and corresponding subband energies. In principle, studying and possibly engineering of these phenomena demand for full atomistic and first principle description of complex interfaces. Moreover, these atomistic configurations should be translated into scattering parameters. These steps are proven to be very challenging [2]. Therefore, any meaningful connection between real interface and transport solvers has been hindered. In this study, critical steps towards establishing such a link are studied by computing the surface roughness of realistic Si/SiO_2 interfaces using first principles density functional theory (DFT). Furthermore, as an application, the detrimental impact of Ge-O bonds on electrical roughness is reported. This is particularly relevant for advanced logic nodes, where SiGe is introduced as channel material [3,4]. Our results show that Ge-residue in oxide can cost severe roughness and potentially hamper the mobility in these devices. The simulations of this work are done by combination of in-house tool and QuantumATK [5].

II. Methodology

To represent the statistics of band transition, the cross section of samples should be large enough. In this report, 3×3 nm² samples with ~3,000 atoms are considered. The interface is prepared by molecular dynamics (MD) steps using ReaxFF

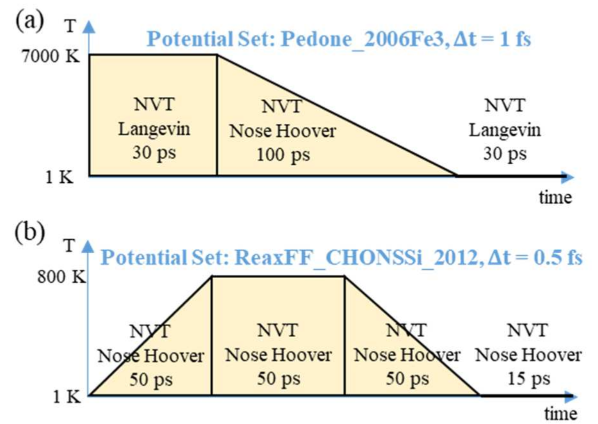

Fig. 1. The molecular dynamics melt-quench profiles. (a) The profile for generating $a\text{-}SiO_2$. (b) The profile for generating $Si/a\text{-}SiO_2$.

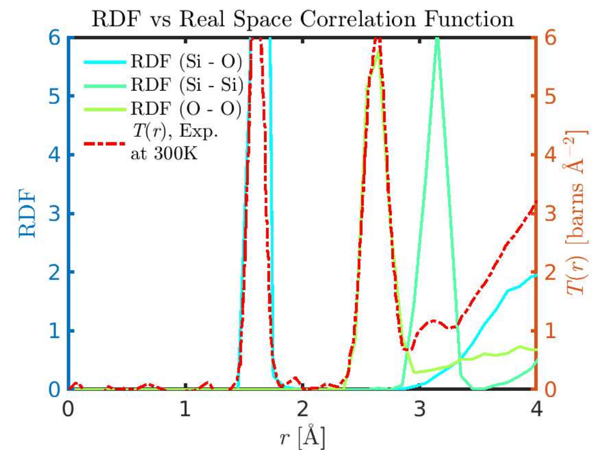

Fig. 2. Radial distribution function (RDF) of simulated $a\text{-}SiO_2$ as compared with the real space correlation, $\boldsymbol{T(r)}$, measurement (red dash-dot line) [6].

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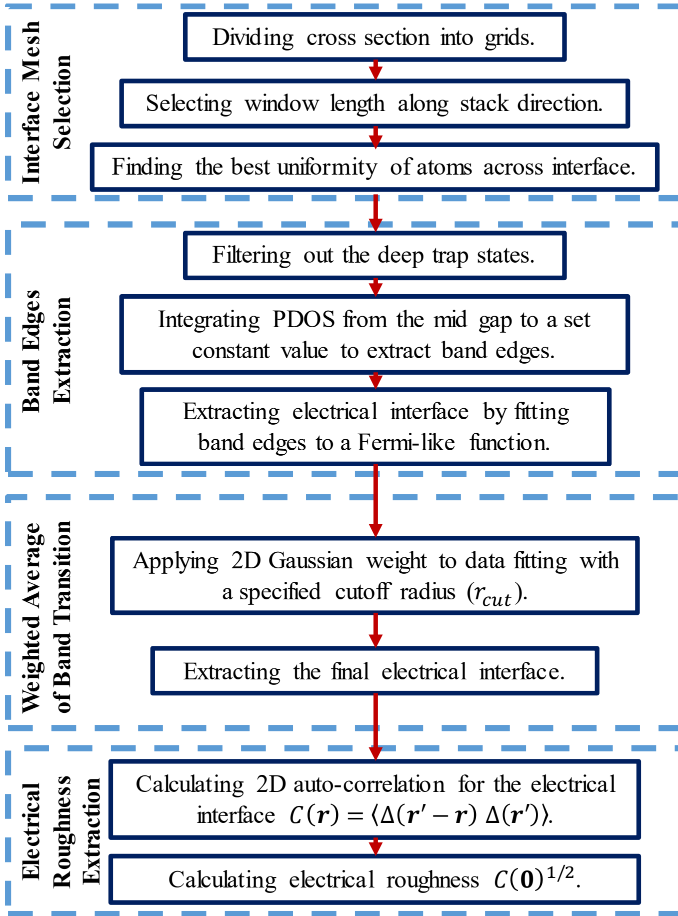

Fig. 3. An algorithm of extracting electrical roughness.

force field [5]. The melt-quench profiles for amorphous SiO_2 (a-SiO_2) and Si/a-SiO_2 systems are shown in Fig. 1. The radial distribution of amorphous sample is in good agreement with experimental data [6], as shown in Fig. 2. To relax the structure, PBEsol functional with double-zeta polarized basis set is used. The density cutoff energy is set to 180 H and pseudopotentials from Refs. [7] and [8] are employed. The gamma point is chosen for density calculation. To calculate projected density of state (PDOS), DFT-1/2 functional [9] is used.

The procedure of extracting electrical roughness is presented in Fig. 3, which can be categorized into 4 sections.

A. *Interface Mesh Selection*

- The cross section is expanded by atomic grids.
- The length of stack is chosen as such that flat band condition is achievable in borders.
- The girds are incrementally displaced to achieve maximum uniformity of atom number in each cell, as shown in Fig. 4.

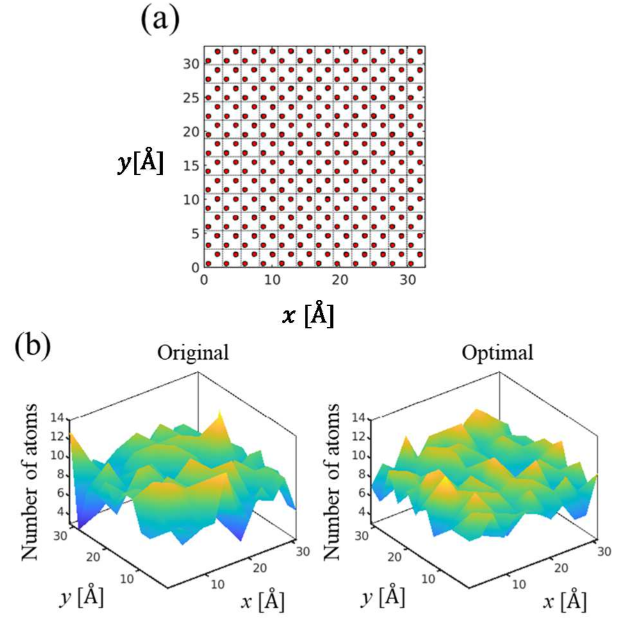

Fig. 4. The selection of interface mesh. (a) 12×12 equally-spacing grids in *x*-*y* plane are selected. This whole mesh is then shifted in this plane such that the standard deviation of the number of atoms in each column is minimal. (b) The distribution of the number of atoms across the interface in the original mesh (left) and in the optimal mesh (right).

B. *Band Edges Extraction*

- The deep trap states in the band gaps are filtered by setting PDOS to zeros between 0.3 eV below and above the mid gaps.
- The values of PDOS below 10^{-4} are filtered out. Therefore, the conduction band (CB) and valence band (VB) edges, E_{edgeC} and E_{edgeV}, respectively, can be extracted, where $Thr = Thr_C = Thr_V = 0.014$,

$$Thr_C = \int_{E_{edgeC}}^{E_C} PDOS(E)dE \qquad (1)$$

$$Thr_V = \int_{E_V}^{E_{edgeV}} PDOS(E)dE \qquad (2)$$

- The band transition along z direction is fitted by Fermi-like function to CB and VB edges

$$CB^{ij}(z) = \alpha_{CB}^{ij} + \beta_{CB}^{ij} \tanh\left(\frac{z - z_{0,CB}^{ij}}{\theta_{CB}^{ij}}\right), \qquad (3)$$

$$VB^{ij}(z) = \alpha_{VB}^{ij} + \beta_{VB}^{ij} \tanh\left(\frac{z - z_{0,VB}^{ij}}{\theta_{VB}^{ij}}\right), \qquad (4)$$

where α^{ij}, β^{ij}, z_0^{ij} and θ^{ij} are fitting parameters, and the indices *ij* refer to grid number in 2D cross section. For each grid, z_0^{ij} is considered as the position of electrical interface.

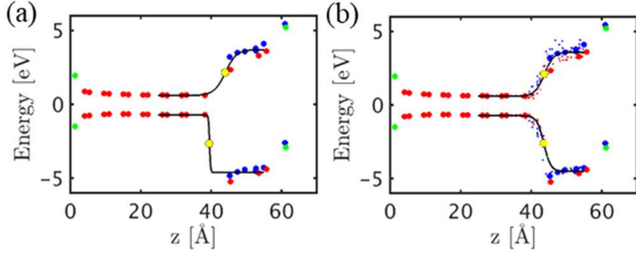

Fig. 5. Extracted band profile and the location of the Si/a-SiO_2 interface for a particular column among the divided columns. (a) Interface position extraction (yellow dots) with equal weight fitting within a given grid column. (b) Interface roughness extraction with Gaussian weight fitting. The small dots correspond to the band edges from neighbor columns within $\boldsymbol{r_{cut}}$. Red dots: Si, blue dots: O, and green dots: H.

Employing this procedure, the fitting parameters in Eqs. (3) and (4) should be collected for all grids. The typical band edges and corresponding fitting for a given atomic columns are shown in Fig. 5. Comparing the fitting curve in Fig. 5 (a) and (b) highlights the impact of adjacent cells. The information of neighboring columns evidently improves the quality of fitting. This may reflect the very nonlocality of energy barrier. In practice, this is implemented by weighted regression, as it is explained in *C* part.

C. Weighted Regression of Band Transition

- Two-dimensional Gaussian weight function ($\mathrm{w}(x, y)$) is applied to data points in regression routine. Here, r_{cut} is set equal to a lattice constant of Si.

$$\mathrm{w}(x, y) = \begin{cases} \exp\left(-\frac{(x-x_{grid})^2}{2\sigma_x^2} - \frac{(y-y_{grid})^2}{2\sigma_y^2}\right), & r_g^2 \le r_{cut}^2 \\ 0, & r_g^2 > r_{cut}^2 \end{cases}, \quad (5)$$

$$r_g^2 = (x - x_{grid})^2 + (y - y_{grid})^2, \quad (6)$$

where $\sigma_x = \sigma_y = \sigma$ is set such that $\mathrm{w}(x, y)$ at r_{cut} is equal to 0.1.

- The final interface positions are obtained by fitting of Eqs. (3) and (4) to the band edges obtained from Gaussian weight.

D. Electrical Roughness Extraction

- The positions of electrical interface are collected for all grids. The corresponding auto-correlation function $C(\boldsymbol{r})$ is subsequently calculated as [2]

$$C(\boldsymbol{r}) = \langle \Delta(\boldsymbol{r'} - \boldsymbol{r})\, \Delta(\boldsymbol{r'}) \rangle, \quad (7)$$

where Δ is the deviation of electrical interface from the average value.

- The electrical roughness is calculated by root-mean-squared height of the electrical interface or $C(\boldsymbol{0})^{1/2}$.

III. Results and Application

Figure 6(a) shows two representative samples of Si/a-SiO_2 and Si/a-SiGeO. For the latter case, 30% of Si atoms in oxide region are randomly replaced by Ge. A subsequent DFT relaxation is then performed. Applying the aforementioned algorithm, the position-dependent electrical interface is extracted in Fig. 6 (b). The 2D auto-correlation function in Eq. (7) is also estimated. The Fourier transform of $C(\boldsymbol{r})$ can be fitted by either exponential or Gaussian function, which are commonly used to model roughness scattering in transport solvers. In Fig. 6 (c), it can be seen that the electrical roughness at Si/a-SiGeO interface is increased significantly as compared with that of Si/a-SiO_2. This is particularly interesting as both interfaces have very similar topography. Nevertheless, Ge-residue triggers higher scattering rate and degrades the electron

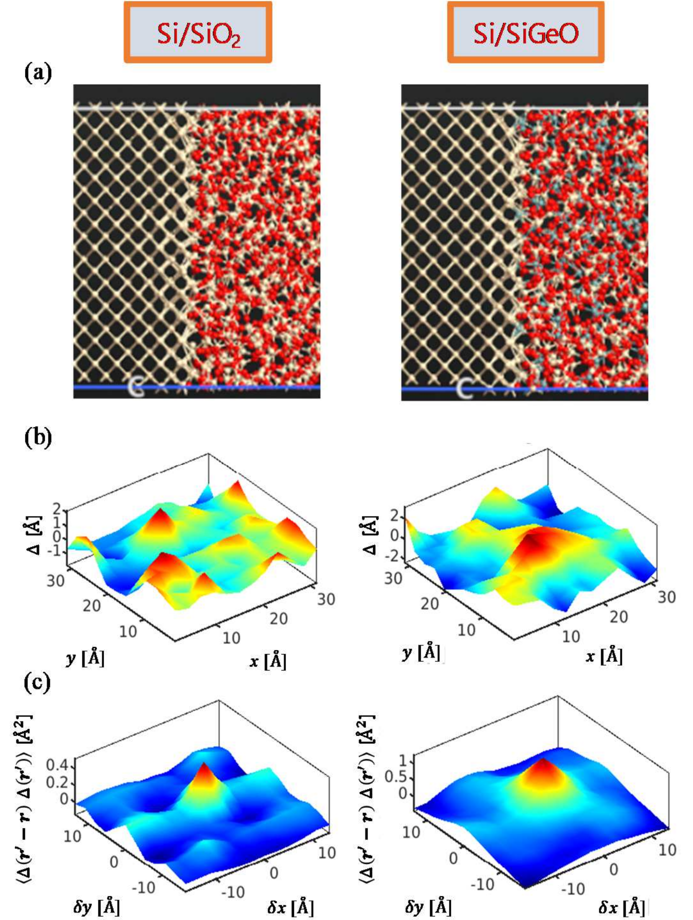

Fig. 6. (a) A schematic view of simulated Si/a-SiO_2 (left) and Si/a-SiGeO (right) with ~3×3 nm^2 cross section of ~3,000 atoms in total. (b) Electrical interface in the conduction bands of Si/a-SiO_2 (left) and Si/a-SiGeO (right). (c) The auto-correlation function for the electrical interface of Si/a-SiO_2 (left) and Si/a-SiGeO (right) in the conduction bands.

mobility. Similar effect has been observed in SiGe FinFET devices. For example in Ref. [3], an additional scattering source near conduction band is reported, which is consistent with our results. Generally, the slope of mobility drop in strong inversion represents the roughness scattering. For SiGe channels, such a slope is steeper than Si devices, e.g. Figs. 6, 8 and 9 in Ref. [3], which concludes larger surface roughness. In case of valance band, Ge-induced roughness is not substantial, as shown in Fig. 7. For SiGe PMOS devices, Ge content induces extra interface state and fixed charges rather than surface roughness. To recover hole mobility, often Si-capping [10] or Ge-pull out should be considered [11]. For all these cases, the notion of high mobility SiGe channel is questionable and can be misleading.

IV. Conclusion

An algorithm to extract the electrical roughness is introduced. Our results show that electrical roughness can be substantially larger than physical roughness resulting from interface topography. The impact of electrical roughness is more pronounced when Ge impurities are presented in oxide region. The extracted root-mean-squared height and auto-correlation function for the electrical roughness can be exported to transport solvers.

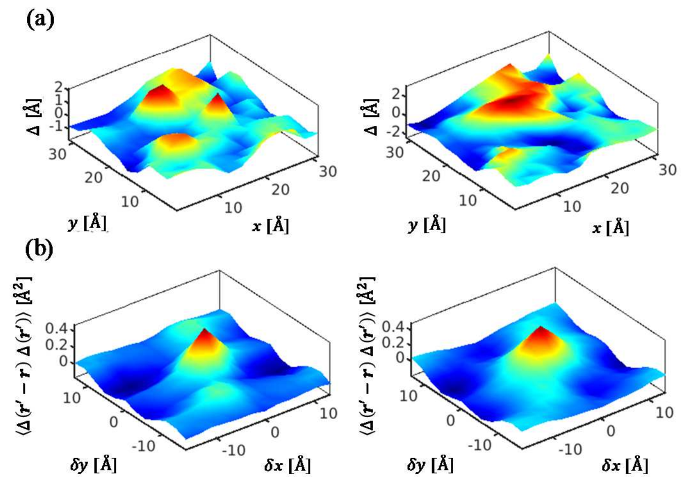

Fig. 7. (a) Electrical interface in the valence bands of Si/a-SiO_2 (left) and Si/a-SiGeO (right). (b) The auto-correlation function for the electrical interface of Si/a-SiO_2 (left) and Si/a-SiGeO (right) in the valence bands.

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