Modeling and Assessment of Atomic Precision Advanced Manufacturing (APAM) Enabled Vertical Tunneling Field Effect Transistor

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***Abstract*— The atomic precision advanced manufacturing (APAM) enabled vertical tunneling field effect transistor (TFET) presents a new opportunity in microelectronics thanks to the use of ultra-high doping and atomically abrupt doping profiles. We present modeling and assessment of the APAM TFET using TCAD Charon simulation. First, we show, through a combination of simulation and experiment, that we can achieve good control of the gated channel on top of a phosphorus layer made using APAM, an essential part of the APAM TFET. Then, we present simulation results of a preliminary APAM TFET that predict transistor-like current-voltage response despite low device performance caused by using large geometry dimensions. Future device simulations will be needed to optimize geometry and doping to guide device design for achieving superior device performance.**

Keywords—atomic precision advanced manufacturing (APAM), tunneling field effect transistor (TFET), band-to-band tunneling, TCAD, Charon

I. Introduction

Atomic precision advanced manufacturing (APAM) is an area-selective doping process wherein phosphine molecules attach to reactive parts of a silicon surface patterned using a scanning tunneling microscope (STM) [1] for atomic precision, or a hard mask for high throughput. Phosphorous (P) dopants are chemically incorporated into the surface of silicon with a 2D sheet density in excess of the solid solubility limit [2], and are buried with a silicon cap layer grown at relatively low temperatures to keep the dopants in place. Though APAM has been widely used to make quantum devices [3] in the past decades, we focus on exploring APAM for opportunities in future microelectronics [4]. Last year, we demonstrated room temperature operation of APAM wires [5], the first step towards microelectronic applications, since previous APAM devices only work at cryogenic temperatures. Recently, we proposed a novel vertical tunneling field effect transistor (TFET) based on APAM [6], as shown schematically in Fig. 1. This APAM TFET has the potential to overcome the two main challenges of conventional TFETs, i.e., low energy efficiency and low on:off current ratios, because of its vertical geometry and atomically abrupt doping profile.

In this paper, we present modeling and assessment of the APAM TFET using TCAD Charon simulation. First, we discuss using TCAD simulation to model the capacitance-voltage (C-V) relation and guide APAM gate stack design. And we discuss how C-V simulations help to understand measured C-V results and infer doping information in a fabricated gate stack. Next, we present simulation results of an initial APAM TFET that predict the TFET indeed shows transistor-like current-voltage behavior despite low device performance, but the low performance can be dramatically improved via geometry dimension optimization. Finally, we summarize our simulation findings and discuss future work.

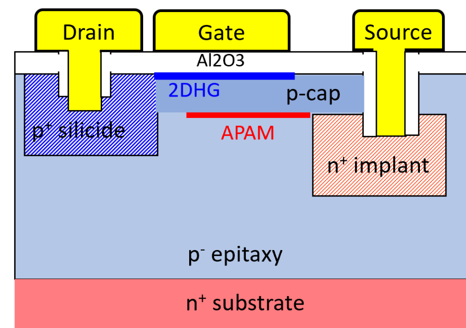

Fig. 1. Cross-sectional schematic (not-to-scale) of the proposed APAM TFET. APAM is used to create the P:δ layer indicated by the red line, which is capped by a p-type cap layer. With a sufficiently negative gate voltage, 2D hole gas is formed at the oxide/p-cap interface; then vertical band-to-band tunneling between 2DHG and APAM wire leads to current flow.

II. Gate Stack C-V Modeling and Measurement

To realize the proposed TFET, one key component is to demonstrate and understand gate control over the channel above an atomically abrupt phosphorus delta (P:δ) layer. This section shows that combination of modeling and experiment clearly demonstrates good gate control in an APAM material stack. To estimate the gate voltages at which holes may accumulate and investigate if hole accumulation occurs before breakdown of either the oxide or silicon material, we simulated the C-V characteristics of an APAM gate stack using Sandia's open-source TCAD code, Charon [7-9]. Simulated C-V curves are plotted in Fig. 2 for different p-cap layer thickness with the gate stack shown as an inset. Clearly, a thicker p-cap layer requires a smaller negative voltage to accumulate holes. For a 15 nm cap layer, hole accumulation occurs around -5 V. For this case, the simulated maximum electric fields in Si and Al_2O_3 are shown in Fig. 3. We observe that the maximum fields in both materials for relevant gate

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This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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voltages are less than their breakdown fields (e.g., Al_2O_3 breakdown field ~ 5 to 30 MV/cm, Si breakdown field ~ a few MV/cm at high doping). Simulations show that hole accumulate can indeed occur in an APAM gate stack before material breakdown. However, there will be a trade-off in device design to achieve reasonable turn-on voltage and sufficiently high current.

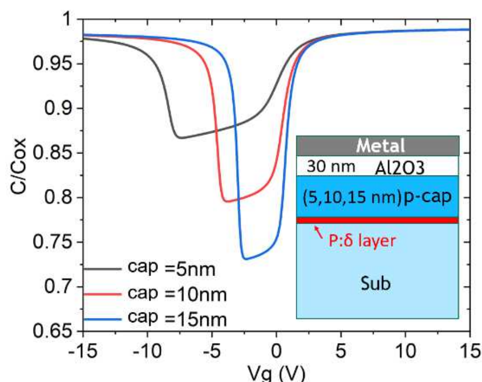

Fig. 2. Simulated C-V curves for an APAM gate stack with different p-cap layer thickness relevant for the APAM TFET shown in Fig. 1.

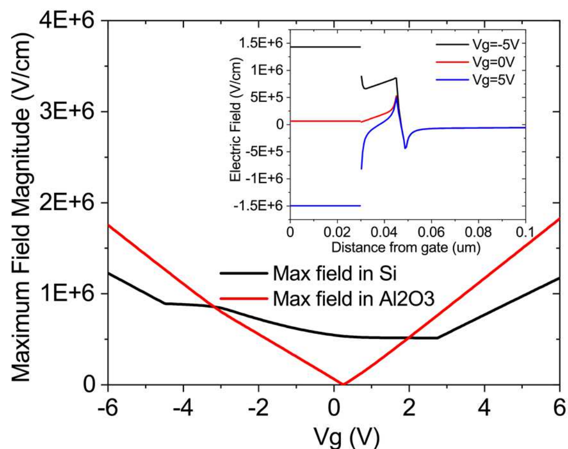

Fig. 3. Simulated maximum electric field magnitude in Si and Al_2O_3 versus gate voltage for the gate stack in Fig. 2 with a 15 nm p-cap layer. Inset: the electric field versus the distance from the gate with the Al_2O_3/Si interface located at 30 nm. Note the fields are discontinuous due to the difference in dielectric constants.

With insight from our simulation study, we have fabricated an APAM gate stack and measured its C-V curves at different frequencies as shown in Fig. 4. The measured results demonstrate that holes can indeed accumulate at sufficiently negative voltages as our simulation suggested. In addition, the frequency dependent characteristics of the measured C-V is significantly different from conventional MOS capacitors. Although the measured gate stack is nominally similar to that in Fig. 5, there was an uncertainty regarding the doping type and value in the cap layer, since variations in the cap growth could change its doping. Normally, a well-controlled cap growth process introduces p-type doping on the order of 10^{18} - 10^{19} cm^{-3}. However, if the cap growth temperature is too high, P dopants in the P:δ layer could diffuse into the cap and turn the doping to n-type at some high value.

To narrow down the cap doping and understand the measured low-frequency C-V, we simulated DC C-V curves for different cap doping types and values as shown in Fig. 5. We found that, the simulated C-V curves (red and magenta) using a p-type cap doping are very different from the measured C-V. To approximately reproduce the measured C-V shape and minimum capacitance, we needed to set the cap doping to n-type with a value of 10^{19} cm^{-3}. Furthermore, to shift the minimum-capacitance voltage close to the measured value, we needed to add fixed negative charges with a density of 1.8×10^{13} cm^{-2} at the oxide/silicon interface. The unexpected n-type cap doping suggested by simulations was later confirmed by SIMS (Secondary Ion Mass Spectroscopy) doping measurements of the APAM gate stack. This indicates that we need tighter control of the cap growth temperature to avoid P diffusion into the cap. Note that the inferred interface charge density of 1.8×10^{13} cm^{-2} is very high, which does not mean there are so many interface charges but represents an effective charge effect. The charges could come from defect charges in the oxide, the cap layer, and/or interfaces.

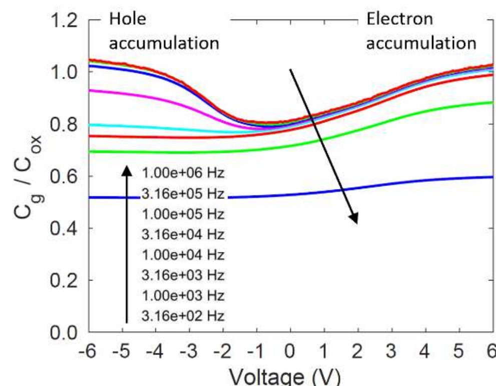

Fig. 4. Measured C-V curves at different frequencies for an APAM gate stack shown in the inset of Fig. 5. It clearly shows hole accumulation at negative voltages and electron accumulation at postive voltages.

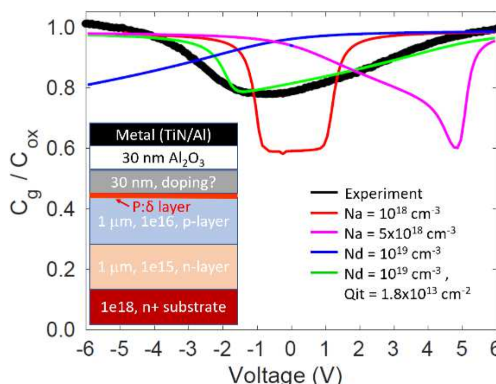

Fig. 5. Simulated DC C-V curves for different cap doping types and values for the gate stack shown in the inset and comparison with the measured low-frequency C-V (black).

For this material stack, we further simulated the C-V curves at higher frequencies, with the results plotted in Fig. 6. The frequency (f) dependence of simulated C-V curves is qualitatively similar to the measured curves, except that the frequency values are different. Moving from a qualitative towards a quantitative comparison will require parameter calibration in the future. The f-dependence of the C-V curves is related to several depletion regions in the stack, as illustrated by the carrier spatial distribution in Fig. 7. At low f, due to thermal generation of carriers, the net capacitance is determined by the capacitance between gate and the P:δ layer, since the P:δ layer screens out other depletion capacitances. At high f, due to lack of carrier generation, the depletion capacitances contribute and they are serially connected, hence leading to smaller net capacitance.

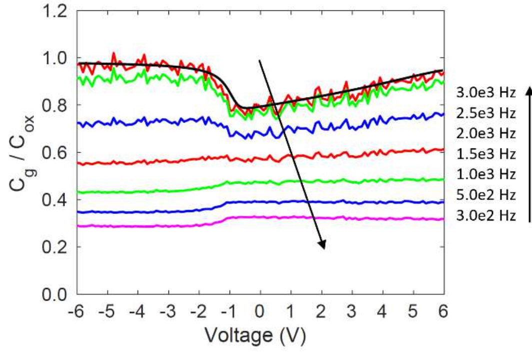

Fig. 6. Simulated C-V curves at different frequencies for the gate stack shown in Fig. 5. The black curve corresponds to the green curve in Fig. 5. Noises in the curves are purely numerical.

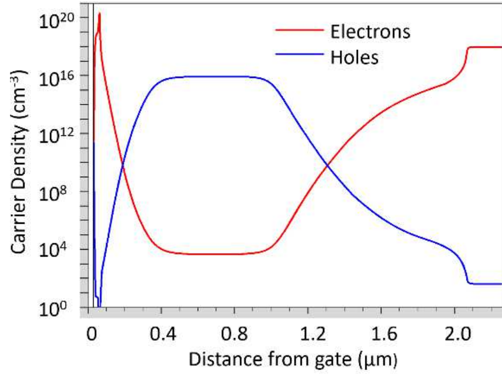

Fig. 7. Simulated carrier densities as a function of the distance from the metal/Al_2O_3 interface at zero gate voltage.

III. APAM TFET Current-Voltage Modeling

The above C-V analysis demonstrates the gate in our material stack confers good control over the channel above the buried P:δ layer, a core component of the APAM TFET. We are currently in the process of fabricating our first set of APAM TFETs. To guide the device design, we used Charon to simulate the current-voltage behavior of the TFET shown schematically in Fig. 8. The choice of the relevant dimensions and doping values in this design were chosen to maximize yield with our traditional photolithography-based device fabrication capability, as opposed to device performance, which we will do in the future.

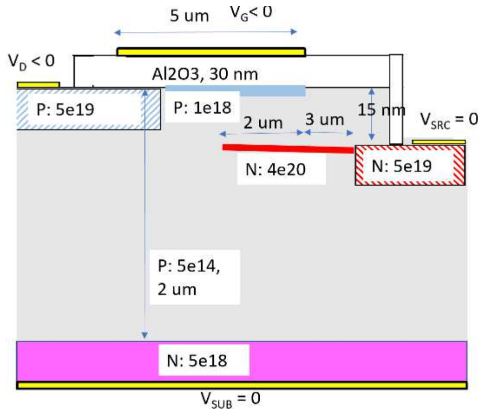

Fig. 8. Schematic of the simulated APAM-TFET (not-to-scale) including relevant dimensions and doping values. The red region denotes the P:δ layer emulated by a 5-nm layer with a donor density of 4×10^{20} cm^{-3}. The yellow rectangles denote where the various electric contacts are located, and they are represented by Ohmic contact boundary conditions in the simulations.

The current flow in the APAM TFET is dominated by band-to-band (B2B) tunneling and can be incorporated in Charon through either the Kane model [10] or the modified Hurkx model [11]. The modified Hurkx model is given by

$$G_{bbt} = AD|F|^{\gamma} e^{-B/|F|} \tag{1}$$

$$D = \frac{n_{ie}^2 - np}{(n+n_{ie})(p+n_{ie})}(1-|\alpha|) - \alpha \tag{2}$$

where G_{bbt} is the electron-hole pair generation rate ($cm^{-3}.s^{-1}$), F is the electric field strength (V/cm), n and p are the electron and hole density (cm^{-3}), respectively, A, B, γ are fitting parameters, and α takes the value of 0, 1, or -1. When α = 0, the original Hurkx model is obtained, which allows both carrier generation and recombination. When α = 1, it allows recombination only; when α = -1, it allows generation only. We found that our simulations using α = 0 lead to difficult convergence and unusual current-voltage curve, which needs to be investigated in the future. Therefore, for all simulation results presented below, we choose to use α = -1, which represents the upper bound of the band-to-band tunneling rate. We note that using α = -1 leads to a small non-zero current at zero drain bias. The vertical electric field from the applied gate voltage and PN junction in the device leads to a non-zero generation rate, which we will discuss further below. In addition to the band-to-band tunneling process, we turned on Fermi-Dirac statistics and band gap narrowing [12] due to the high doping. We further utilized the doping dependent Arora mobility model [13], and turned on Auger and Shockley-Read-Hall (SRH) recombination with concentration dependent carrier lifetime [14].

The simulated drain current (I_D) vs. drain voltage (V_D) curves at different gate voltages are shown in Fig. 9(a), and the simulated drain current vs. gate voltage curves at different drain voltages are given in Fig. 9(b). The simulated curves clearly show transistor-like responses despite low drain currents and high gate voltages. The gate threshold voltage is about -6 V as seen from Fig. 9(b), which is consistent with the blue C-V curve in Fig. 2 that shows full hole accumulation at the Al_2O_3/Cap interface occurs around -6 V. Fig. 9(a) shows that, for drain voltages between 0 and -1 V, the drain currents are at the noise level; for more negative drain voltages, the drain currents first increase rapidly with drain voltages and then show much smaller increase with increasing negative drain voltages.

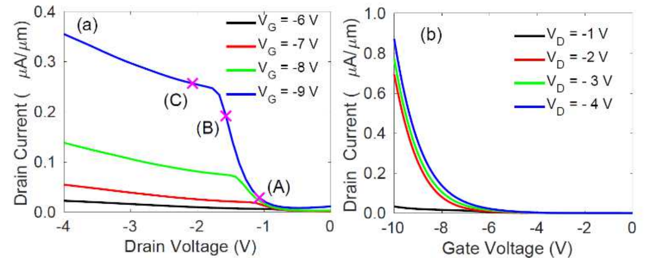

Fig. 9. (a) Simulated I_D-V_D curves at different gate voltages. (b) Simulated I_D-V_G curves at different drain voltages for the device shown in Fig. 8.

To understand the simulated I_D-V_D response, we plotted the electric field spatial distribution in Fig. 10 in the region where the 2DHG layer and the P:δ layer are overlapped for the three drain voltage points denoted as (A), (B), and (C) in Fig. 9(a). We see that, given a fixed V_G of - 9 V, as the drain voltage increases from point (A) to point (B), the electric field in the Al_2O_3 region reduces, while the field in the p-cap layer

increases. However, when the drain voltage increases from point (B) to point (C), the electric fields in the Al_2O_3 and cap regions show very little change. The decreasing field in the Al_2O_3 region with increasing negative V_D is because more negative V_D reduces the field effect of a fixed V_G. The field in the cap layer, meanwhile, is strongly influenced by the increasing lateral field with increasing V_D between source and drain. Nevertheless, once the current reaches some level, there are so many carriers that screening slows down the field effect, which is why the increase of current is much weaker from (B) to (C). The electric field distribution directly determines the B2B tunneling rate, as shown in Fig. 11 for the corresponding drain voltages. As expected, the B2B tunneling occurs mainly in the cap layer. The larger increase in B2B tunneling with increasing V_D from (A) to (B) than from (B) to (C) is responsible for the sharper increase in the drain current from (A) to (B).

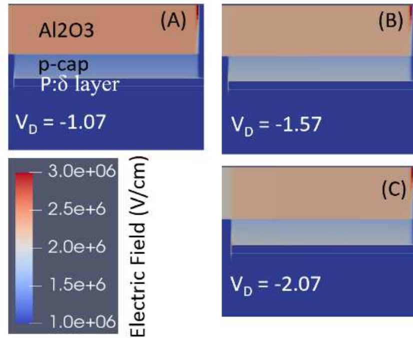

Fig. 10. Electric field distribution in the region where the Al_2O_3 oxide, p-cap, P:δ layers are overlapped for V_G = -9 V and three drain voltage points denoted by (A), (B), and (C) in Fig. 9(a).

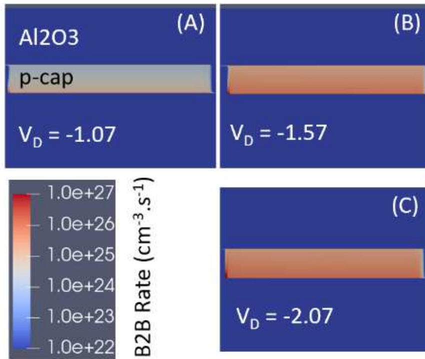

Fig. 11. Band-to-band tunneling rate distribution in the region where the Al_2O_3 oxide, p-cap, P:δ layers are overlapped for V_G = -9 V and three drain voltage points denoted by (A), (B), and (C) in Fig. 9(a).

The above simulation results predict that the proposed APAM TFET will produce transistor-like response, even with unusual device dimensions chosen to simplify fabrication for our in-house capabilities. We observe the simulated device performance (e.g., on current, gate threshold voltage) for this big TFET device is far from being competitive with state-of-the-art FinFETs [15] or lateral TFETs [16]. However, there are many geometry dimensions (e.g., oxide thickness, cap thickness, cap doping, etc.) that can be optimized to achieve much better performance. As an example, we reduced the Al_2O_3 oxide thickness from 30 nm to 20 nm, while keeping all other dimensions the same as in Fig. 8. The simulated I_D-V_D curves for this case are shown in Fig. 12, where the drain currents for drain voltages more negative than -1 V are nearly ten times of those in Fig. 9(a), even though only the oxide thickness is reduced. For drain voltages between 0 and -1 V, we are not confident about the simulation results, because of the non-zero B2B tunneling at zero/near zero drain bias, which needs further investigation in the future. As a second study case, we reduced the p-cap layer thickness (above the P:δ layer) from 15 nm to 10 nm, while keeping all other dimensions the same as in Fig. 8, with the simulation results given in Fig. 13. Compared to Fig. 9(a), the drain currents in Fig. 13 are significantly higher and the currents start flowing at smaller negative drain voltages due to the thinner p-cap layer. Clearly, optimization of APAM TFET geometry dimensions has the potential of achieving superior device performance.

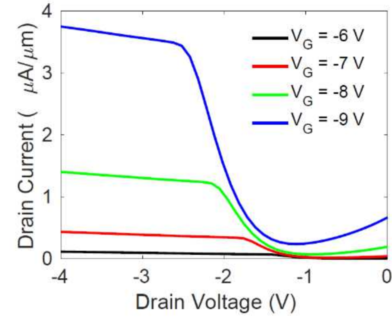

Fig. 12. Simulated I_D-V_D curves at different gate voltages for a device identical to that in Fig. 8 except the Al_2O_3 oxide thickness is reduced from 30 nm to 20 nm.

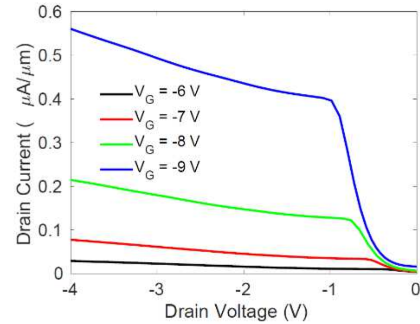

Fig. 13. Simulated I_D-V_D curves at different gate voltages for a device identical to that in Fig. 8 except the p-cap layer thickness is reduced from 15 nm to 10 nm.

IV. CONCLUSIONS

We have presented simulation results and discussions of recently proposed APAM enabled vertical TFET. We showed that, via combination of simulation and experiment, we achieved good gate control of the channel on top of a buried P:δ layer, an essential component of the TFET. We presented the simulated current-voltage responses of a preliminary APAM TFET that clearly show transistor-like behavior through the vertical band-to-band tunneling process. We also showed that the TFET device performance can be dramatically improved by adjusting some of the geometry dimensions. We plan to optimize APAM TFET geometry and doping via extensive TCAD simulations to guide device design with the goal of achieving superior device performance. As part of this effort, we will investigate ways of improving the band-to-band tunneling model to address the non-zero tunneling issue at zero bias and to achieve robust simulation convergence.

REFERENCES

[1] F. J. Ruess, L. Oberbeck, M. Y. Simmons, K. E. J. Goh, A. R. Hamilton, T. Hallam, et al., “Toward atomic-scale device fabrication in silicon using scanning probe microscopy,” Nano Letters, vol. 4, no. 10, pp. 1969–1973, 2004.

[2] F. Mazzola, C-Y. Chen, R. Rahman, X.-G. Zhu, C. M. Polley, T. Balasubramanian, P. D. King, P. Hofmann, J. A. Miwa, and J. W. Wells, “The subband structure of atomically sharp dopant profiles in silicon,” npj Quantum Mater., vol. 5, article no. 34, 2020.

[3] Y. He, S. K. Gorman, D. Keith, L. Kranz, J. G. Keizer, and M. Y. Simmons, “A two-qubit gate between phosphorus donor electrons in silicon,” Nature, vol. 571, pp. 371-375, 2019.

[4] D. R. Ward, S. W. Schmucker, E. M. Anderson, E. Bussmann, L. Tracy, T. Lu, et al., “Atomic precision advanced manufacturing for digital electronics,” Elec. Dev. Fail. Anal. vol 22, pp. 4-10, 2020.

[5] X. Gao, L. Tracy, E. M. Anderson, D. M. Campbell, J. A. Ivie, T. Lu, D. Mamaluy, S. W. Schmucker, and S. Misra, "Modeling Assisted Room Temperature Operation of Atomic Precision Advanced Manufacturing Devices," 2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 277-280, 2020.

[6] T.-M. Lu, X. Gao, et al., “Path towards a vertical TFET enbled by atomic precision advanced manufacturing,” oral presentation at the Silicon Nanoelectronic Workshop, All-Virtual, June 2021, Japan.

[7] *Charon: Parallel TCAD Simulation*. Accessed: July 26, 2021. [Online]. Available: https://charon.sandia.gov/.

[8] X. Gao, D. Mamaluy, P. R. Mickel, and M. Marinella, “Three-dimensional fully-coupled electrical and thermal transport model of dynamic switching in oxide memristors,” ECS Trans., vol. 69, no. 5, pp. 183–193, Oct. 2015.

[9] X. Gao, B. Kerr, and A. Huang, “Analytic band-to-trap tunneling model including band offset for heterojunction devices,” J. Appl. Phys., vol. 125, no. 5, Art. no. 054503, Feb. 2019,

[10] E. O. Kane, “Zener tunneling in semiconductors,” J. Phys. Chem. Solids, vol. 12, pp. 181-188, 1959.

[11] G. A. M. Hurkx, D. B. M. Klaassen, M. P. G. Knuvers, “A new recombination model for device simulation including tunneling,” IEEE Trans. Electron Dev., vol. 39, no. 2, pp. 331–338, 1992.

[12] J. W. Slotboom, “The pn production in silicon,” Solid-State Electron., vol. 20, pp. 279-283, 1977.

[13] N. D. Arora, J. R. Hauser, D. J. Roulston, “Electron and hole mobilities in silicon as a function of concentration and temperature,” IEEE. Trans. Electron Devices, vol. 29, no. 2, pp. 292-295, 1982.

[14] X. Gao, Q. Looker, T. J. Web, K. R. DePriest, and B. Ulmen, “Simulation and modeling of time-resolved X-ray detector for the Saturn accelerator,” IEEE Nucl. Sci., vol. 68, no. 7, pp. 1454–1464, Jul. 2021.

[15] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, “Exploring sub-20nm FinFET design with Predictive Technology Models”, DAC Design Automation Conference 2012, pp. 283-288, 2012.

[16] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," in IEEE Journal of the Electron Devices Society, vol. 2, no. 4, pp. 44-49, Jul. 2014.