A Sub-k_BT/q Dirac-source Graphene Nanoribbon Field-effect Transistor

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***Abstract*—A sub-k_BT/q Dirac-source (DS) graphene nanoribbon FET has been studied using a coupled mode-space non-equilibrium Green function solver employing *k·p* electronic structures. A 13 dimer wide armchair graphene nanoribbon (13-AGNR) FET connected to a semimetallic 162-AGNR source contact is simulated to study the physics of a proposed DSFET design. Density-of-states filtering at the source contact is explored by shifting its Fermi level via variations on doping concentration. An optimized design achieves a minimum subthreshold swing (SS) of 42 mV/dec and sub-60mV/dec operation across three orders of I_D magnitude.**

Keywords-Dirac source, graphene nanoribbon, Sub-k_BT/q, DoS filtering, ultra-low V_{DD} applications

I. INTROUDUCTION

A sub-k_BT/q transistor enables power supply reduction and improves energy efficiency in logic circuits. Among candidates, tunneling FETs (TFETs) suffer severe drive current (I_{ON}) penalties while negative capacitance FETs (NCFETs) exhibit large hysteresis within their steep-slope operation range. A Dirac-source FET (DSFET) [1, 2] is a promising alternative where density-of-states (DoS) engineering involves using a Dirac semi-metal source-contact to filter thermionic leakage (I_{OFF}), thus allowing sub-60mV/dec operation without sacrificing I_{ON}. In this work, a 13 dimer wide armchair graphene nanoribbon (13-AGNR [3]) FET connected to a semimetallic 162-AGNR source contact is simulated to study the physics of a proposed DSFET design. DoS filtering at the source contact is explored by shifting its Fermi level via variations on doping concentration. Finally, an optimized design yields a minimum subthreshold swing (SS) of 42 mV/dec and sub-60mV/dec operation across three orders of I_D magnitude.

II. METHODOLOGY

To achieve computationally-efficient simulations of DSFETs, a coupled mode-space non-equilibrium Green function (NEGF) solver employing ***k·p*** electronic structures for AGNRs has been developed [4]. A Wilson's mass term is introduced to achieve desired boundary conditions on Dirac-like Hamiltonians [5]. Further corrections on boundary conditions allow accounting for finite-size effects and yield the correct band gap sequence with varying AGNR width [5, 6]. Simulation parameters have been chosen to reproduce band gaps from density functional theory (DFT) simulations employing the generalized-gradient approximation (GGA), as shown in Fig. 1. While DFT is well known to underestimate band gap magnitudes, our simulations serve as proof-of-concept and allow exploring the physics behind electronic transport in AGNR-based DSFETs.

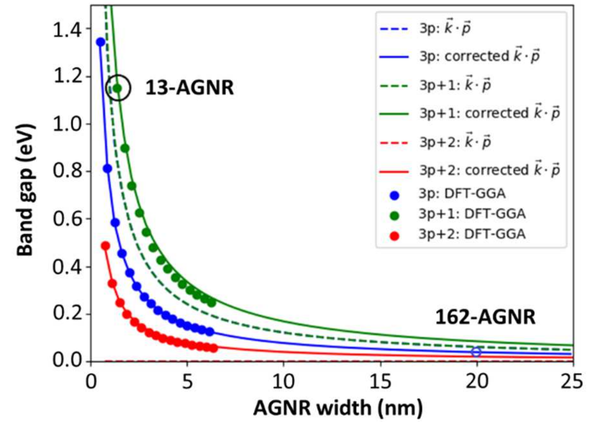

Fig. 1 Band gap vs. AGNR width for 3p, 3p+1, and 3p+2 dimer lines. The symbols show the simulation results from DFT-GGA. The dashed lines represent the ***k·p*** results without corrections on boundary conditions. The solid lines are the ***k·p*** results with the boundary condition corrections [5, 6]. The ***k·p*** model (*i.e.*, the solid lines) employed in the NEGF solver [4] shows a good agreement with the DFT results. Finally, the design points of 13- and 162-AGNRs for the AGNR-based DSFETs are labeled in the figure.

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The transistor is designed as *n*-type using a 13-AGNR, which exhibits a band gap comparable to that of silicon (*i.e.*, E_G=1.12 eV). The undoped channel length is 15 nm, the n^+-drain extension is 10 nm, and the n^+-source extension is 5 nm. The AGNR dielectric constant is 6.9 [7]. The equivalent oxide thickness (EOT) is 1 nm, which covers the channel and the n^+-source extension. A 162-AGNR with a band gap of 10 meV is connected to the n^+-source of the 13-AGNR-FET. Three doping concentrations (Ns=10^{13}, -5×10^{12}, -10^{13} cm^{-2}) are considered at the 162-AGNR source contact. To prevent abrupt potential change at the p^+-n^+ junction and improve numerical convergence, a 5 nm *i*-region is inserted between the p^+-n^+ junction. A double-gate device structure with the wide source reservoir and band structures for the 13- and 162-AGNRs are shown in Fig. 2.

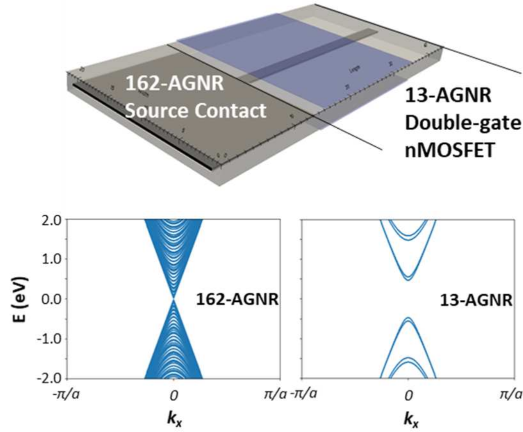
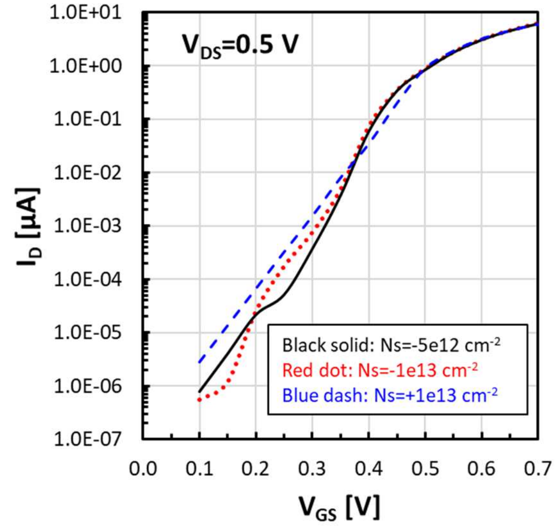


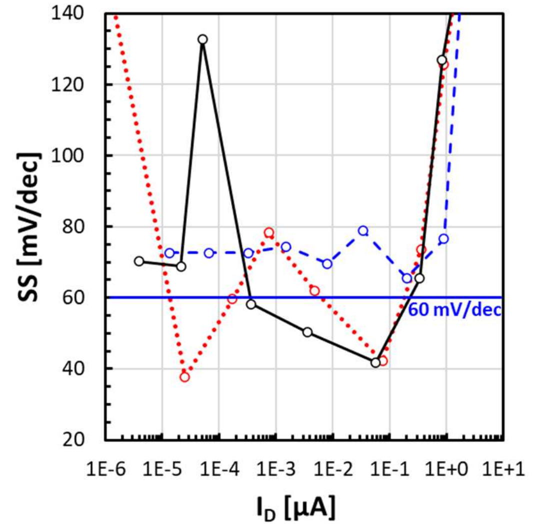
Fig. 2 A schematic device structure of the DSFET and the electronic structures (E *vs*. k_x) of 13- and 162-AGNRs are plotted. A 162-AGNR shows a bandgap of 10 meV, which exhibits semimetallic properties at room temperature. A 13-AGNR shows a bandgap of ~1.15 eV, which demonstrated semiconductor properties.

III. RESULT AND DISCUSSION

To study variations in the DoS near the n^+-type source's Fermi-level, three doping concentrations (Ns=10^{13}, -5×10^{12}, -10^{13} cm^{-2}) are considered at the 162-AGNR source contact. One is *n*-type (*i.e.*, Ns=10^{13} cm^{-2}) and the remaining two are *p*-type (*i.e.*, Ns=-5×10^{12}, -10^{13} cm^{-2}). Fig. 3 shows the transfer characteristics (I_D-V_{GS}) and the subthreshold slope ($SS \equiv [\partial \log_{10}(I_D)/\partial V_{GS}]^{-1}$) versus the drain current for these three scenarios. The black solid and red dot lines show *p*-type source contacts with Ns=-5×10^{12} and -10^{13} cm^{-2}, respectively. The blue dashed line shows *n*-type source contact with Ns=10^{13} cm^{-2}. All designs exhibit similar drive current at the ON state (I_{ON}), confirming that tunneling from 162-AGNR to 13-AGNR is almost transparent. The case with an *n*-type source contact results in standard MOSFET behavior with SS>60 mV/dec. On the contrary, sub-60mV/dec SS has been demonstrated for cases with *p*-type source contacts.



(a)



(b)

Fig. 3 (a) I_D-V_{GS} and (b) SS vs. I_D for V_{DS}=0.5 V with different doping concentrations on the 162-AGNR source contact. The black solid and red dot lines show *p*-type source contact with 5×10^{12} and 10^{13} cm^{-2}, respectively. The blue dashed line shows *n*-type source contact with 10^{13} cm^{-2}.

To understand the underlying physics, the band diagrams with local DoS (LDOS) and energy-resolved current for *n*-type and *p*-type source contacts are plotted at V_{GS}=0.4 and V_{DS}=0.5 V in Fig. 4. Both have the same doping concentration of 10^{13} cm^{-2} but with different types. The device with *p*-type source contact shows an energy-resolved current density profile sharper than that of the device with *n*-type source contact. The DoS filtering of the Dirac source suppresses high energy tails for carrier injection and results in an improved SS of 42mV/dec for the device with *p*-type source contact *vs*. ~70mV/dec for the device with *n*-type source contact.

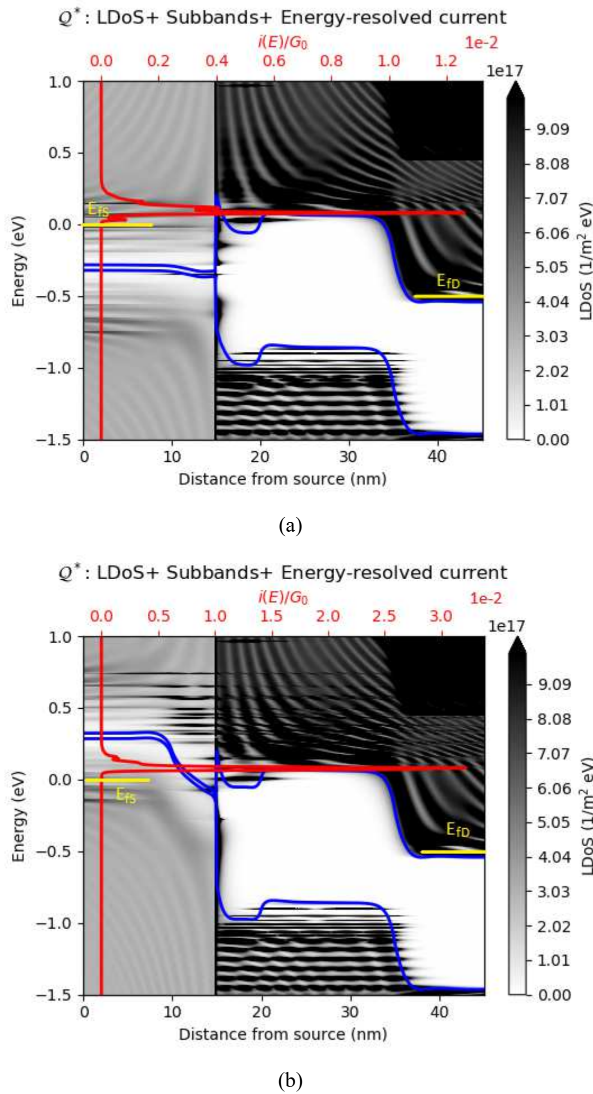


Fig. 4 The band diagrams with LDOS and energy-resolved current for (a) *n*-type and (b) *p*-type source contacts are plotted at V_{GS}=0.4 and V_{DS}=0.5 V. Both have the same doping concentration of 10^{13} cm^{-2} but with different types.

In addition to the difference between *n*- and *p*-type source contact, the design with Ns=-10^{13} cm^{-2} interestingly shows two steps with sub-60mV/dec SS. Fig. 5 shows the same plot but extracted at V_{GS}=0.2 and V_{DS}=0.5 V for the device. The 1st and 2nd sub-60mV/dec shown in Fig. 5 and Fig. 4 (b) occur as a consequence of DoS filtering when the channel band edge either aligns with the source contact's band gap, or gets to be $3k_BT$ below the source contact's valence band edge [8]. Reducing the doping concentration (*i.e.*, Ns=-5×10^{12} cm^{-2}) in the source contact shifts the 1st alignment towards larger values of V_{GS} and allows concatenation of both sub-60mV/dec swings, resulting in an optimized design with sub-60mV/dec over 3 orders of magnitude in I_D and a minimum subthreshold swing (SS) of 42 mV/dec, as illustrated in Fig. 3.

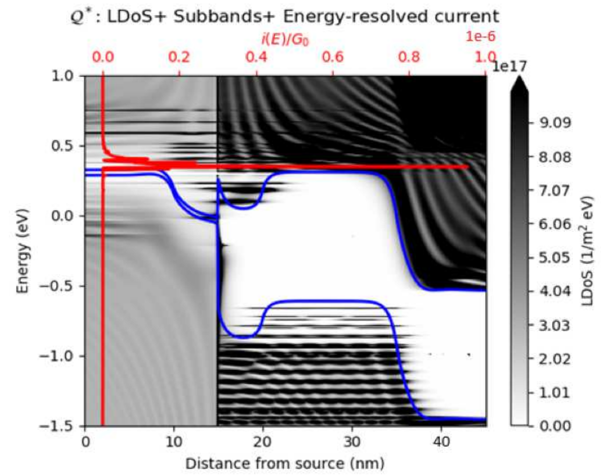


Fig. 5 Band diagrams with LDoS and energy-resolved current extracted at V_{GS}=0.2 V and V_{DS}=0.5 V for the DSFET with 10^{13} cm^{-2} *p*-type source contact (Ns=-10^{13} cm^{-2}).

Finally, potential current gain over a normal MOSFET and preferred operation voltage (V_{DD}) for the optimized design need to be quantified. Since the case with an *n*-type source contact results in standard MOSFET behavior with SS>60 mV/dec, the device with the *n*-type source contact is taken as reference. Fig. 6 (a) shows the transfer characteristics centered at I_{OFF}=100 pA for the devices with *n*-type source contact (blue dashed line, Ns=10^{13} cm^{-2}) and the optimized design (black solid line, Ns=-5×10^{12} cm^{-2}). The current ratio at V_{DS}=0.5 V is plotted in Fig. 6 (b). The optimized design has ~10× current gain at V_{GS}=0.2 V. Since the drain-induced barrier lowering (DIBL) is

quite small for the optimized design shown in Fig. 6 (a), different V_{DS} of 50 mV and 0.5 V do not modify the current level significantly. Therefore, results show that the optimized design is suitable for ultra-low V_{DD} applications at V_{DD}=0.2 V.

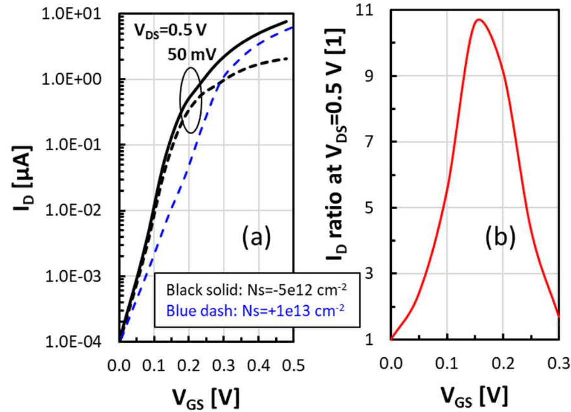


Fig. 6 (a) I_D-V_{GS} for the devices with *n*-type source contact (blue dashed line) and the optimized design (black solid line) at V_{DS}=0.5 V. The black dashed line shows I_D-V_{GS} at V_{DS}=50 mV for the optimized design, which demonstrates small DIBL in the optimized design. (b) The I_D current ratio at V_{DS}=0.5 V.

IV. CONCLUTION

In summary, sub-60mV/dec swing has been observed in AGNR-based DSFET designs due to DoS filtering mechanisms exploiting the presence of a band gap in the source contact, and its linear dispersion. The optimized design of the 13-AGNR-FET gives a minimum subthreshold swing (SS) of 42 mV/dec and sub-60mV/dec over three orders of I_D magnitude, which is suitable for ultra-low V_{DD} applications at V_{DD}=0.2 V.

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