Quantum Transport Simulations of Short Channel Effects Induced by Domain Interactions in Ferroelectric FETs

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***Abstract*—We present a phase-field based quantum transport study on the effect of the polarization multi-domain in the ferroelectric field-effect transistors (FE-FETs). The behavior of FE-FETs is simulated by self-consistently solving the nonequilibrium Green's functions for carrier transport, Landau-Khalatnikov equations for polarization behavior with domain interactions, and Poisson's equations for the electrostatics of the whole device. We found that the drain-induced barrier lowering (DIBL) can be reduced in the case of FE-FETs, compared to the conventional MOSFETs with the high-κ dielectric (HK FETs). As the gate length decreases, DIBL is more reduced, and so FE-FETs show significant performance improvement for short scaled devices, compared to HK FETs. We also found that the double-barrier-like channel potential profile can be induced by the multi-domain configuration. This gives rise to the direct source-to-drain tunneling leakage, causing the abrupt performance degradation. However, for extremely scaled FE-FETs, the polarization bound charge effect is weakened due to the reduction of the domain width, making the abrupt performance degradation disappear.**

***Index Terms*—ferroelectric FETs, domain interaction, short channel effect, quantum transport**

I. Introduction

Ferroelectric field-effect transistors (FE-FETs) have attracted much attention for next-generation steep-slope logic devices since the recent discovery of the ferroelectricity in doped-HfO_2 which is compatible with the conventional CMOS process [1]–[3]. Recent phase-field studies for long channel FE-FETs have reported that as thickness of ferroelectric layer (T_{FE}) decreases, the performance is improved due to the enhanced permittivity caused by the dense polarization (P) multi-domain [4]–[6]. However, few works have been reported on the impact of the multi-domain on the performance of FE-FETs for short channel devices at sub-10 nm scale. Since P multi-domain can affect the channel potential in scaled devices, it is important to investigate the performances of the short channel devices in the presence of the multi-domain.

In this work, we present a phase-field based quantum transport study on the multi-domain effects in the double-gate (DG) FE-FETs with short channel lengths. The two kinds of FE-FETs, single-stacked FE (S-FE) FETs and double-stacked FE (D-FE) FETs, are investigated to explore the P multi-domain effects. Conventional DG MOSFETs with high-κ dielectric (HK FETs) are also simulated and compared to FE-FETs. The potential of FE FETs at sub-10 nm sclae is assessed in this work. We analyze the on-current (I_{ON}) and the

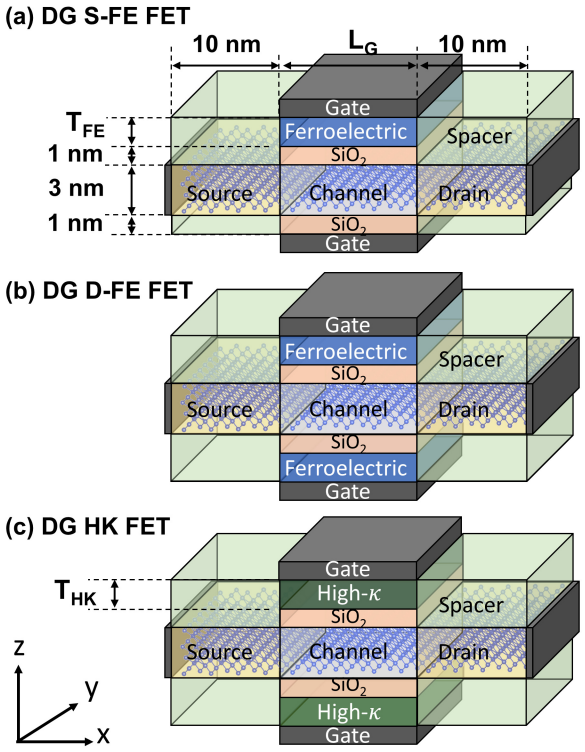

Fig. 1. Schematics of the simulated double gate (DG) FETs: (a) single ferroeletric-stacked FETs (S-FE FETs), (b) double ferroelectric-stacked FETs (D-FE FETs), and (c) high-κ FETs (HK FETs). For all devices, the channel thickness is 3 nm and the thickness of the interlayer dielectric (SiO_2) is 1 nm. The dielectric constant of the spacer is 3.9. The dielectric constants in the FE layer (background permittivity) and the high-κ oxide are 16 and 25, respectively.

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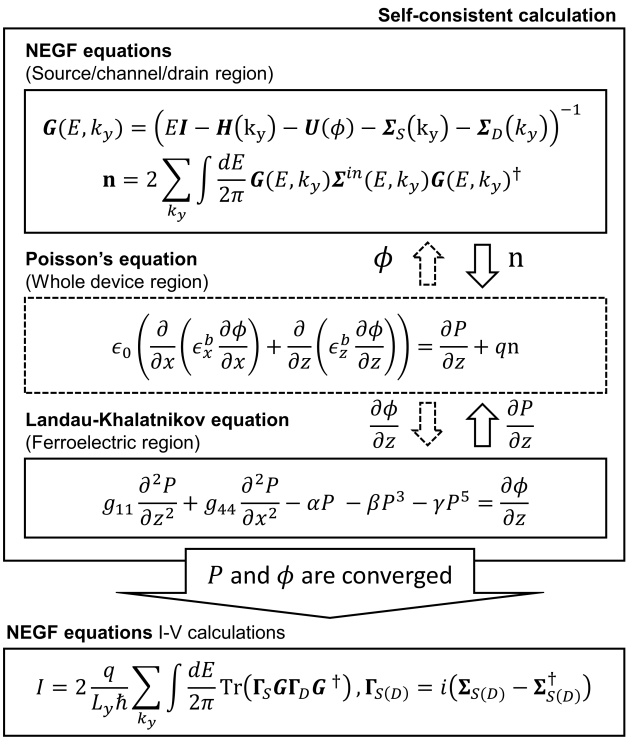

Fig. 2. Overall simulation flow. The three equations of NEGF equations, Poisson's equation, and Landau-Khalatnikov equation with domain interaction terms are self-consistently solved.

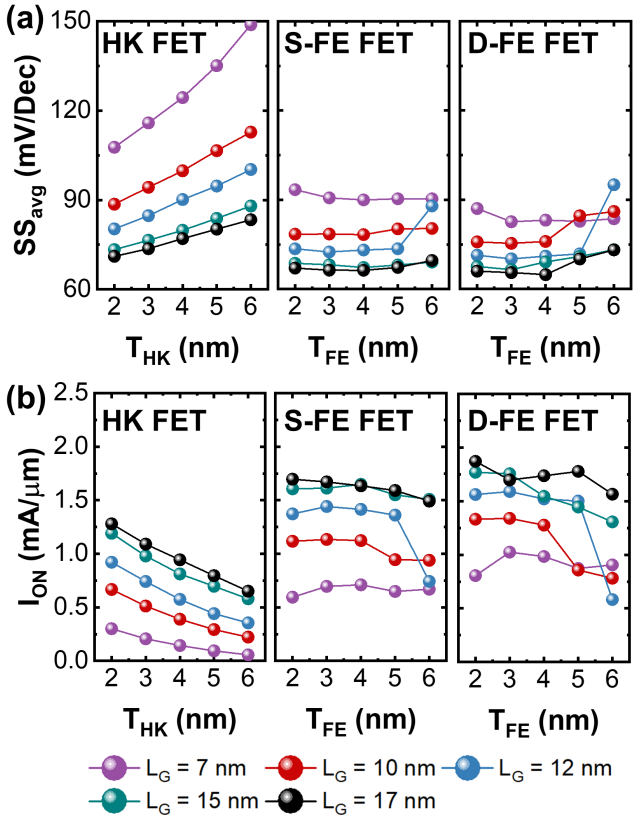

Fig. 3. (a) I_{ON} and (b) SS_{avg} for high-κ FETs, S-FE FETs, and D-FE FETs as functions of the thickness of the thickness of the high oxide (T_{HK}) and the ferroelectric layer (T_{FE}).

average subthreshold swing (SS_{avg}) as T_{FE} and gate length (L_G) are varied.

II. Simulation Methods

We simulated silicon DG FE-FETs and HK FETs with channel thickness of 3 nm as shown in Fig. 1, where the current flows along [100] direction. T_{FE} for FE-FETs and the thickness of the high-κ dielectric (T_{HK}) for HK FETs are varied from 2-6 nm. L_G is scaled down from 17 nm to 7 nm. All the simulations are conducted at the temperature of 300 K with a supply voltage (V_{DD}) of 0.4 V. The doping density of the source and drain regions is 1×10^{20} cm^{-3}, and the channel region is undoped. Threshold voltage (V_{TH}) is defined as the gate-to-source voltage (V_{GS}) such that the drain current (I_D) is equal to OFF-state current (I_{OFF}) of 0.1 A/m. I_{ON} is evaluated at V_{GS} = V_{TH} + V_{DD}. SS_{avg} is obtained over three orders of magnitude of I_D from I_{OFF}.

The overall simulation procedure is shown in Fig. 2. The transport properties of the baseline FETs are treated with nonequilibrium Green's function (NEGF) using sp^{3}d^{5}s* tight-binding (TB) Hamiltonians. Ballistic transport is assumed for the calculation of the carrier density and current. For efficient NEGF calculations, the size of TB Hamiltonians is reduced using the mode space method without the loss of the accuracy in terms of device transport simulations [7]. The behavior of P in the FE layer is described by the Landau-Khalatnikov (LK) equation at static condition including domain interactions along the x- and z-directions [8]. In this work, we assumed P direction is perpendicular to the gate contact (z-direction). The assumption is justified because the direction of P can be experimentally fixed under a compressive strain [5]. To capture the electrostatic effect of the discontinous P at the interface between the FE layer and the interlayer dielectric (DE), the bound charge density ($-dP/dz$) is included in the Poisson's equation. For the simulation of the DG FE-FETs operation, we self-consistently solved the Poisson's equation, multi-domain LK equation, and NEGF equations until the electrostatic potential and P are converged. The parameters of the Landau coefficients and domain interaction terms were taken from [4].

III. Results and Discussion

DG FE-FETs show improved performances compared to DG HK FETs. Figs. 3(a) and (b) show I_{ON} and SS_{avg} of DG FE-FETs and DG HK FETs for various L_G as functions of T_{FE} and T_{HK}, respectively. It is shown that for FE-FETs, SS_{avg} is lower and I_{ON} is higher than those of HK FETs at the same L_G and thickness (T_{FE} = T_{HK}). For example, at L_G = 17 nm and T_{FE} = T_{HK} = 2 nm, D-FE FET exhibits SS_{avg} of 66 mV/dec and I_{ON} of 1.87 A/m, while SS_{avg} and I_{ON} of HK FET are 71 mV/dec and 1.28 A/m, respectively. The performance improvement agrees well with the recent

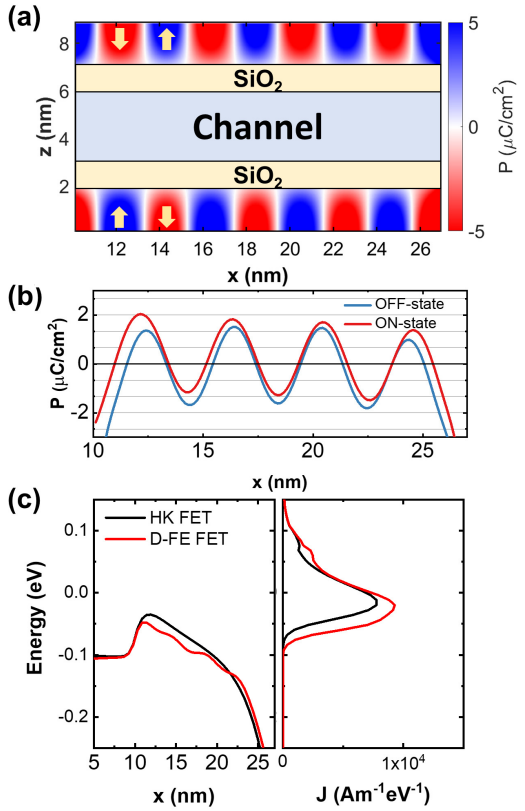

Fig. 4. (a) P configuration of D-FE FETs at OFF-sttate and (b) P profiles at the interface between FE and DE layers along the channel at ON- and OFF-state with L_G = 17 nm and T_{FE} = 2 nm. The yellow arrows indicate the P directions. (c) Conduction band edge profiles of HK FET and D-FE FET at ON-state and the current densities (J).

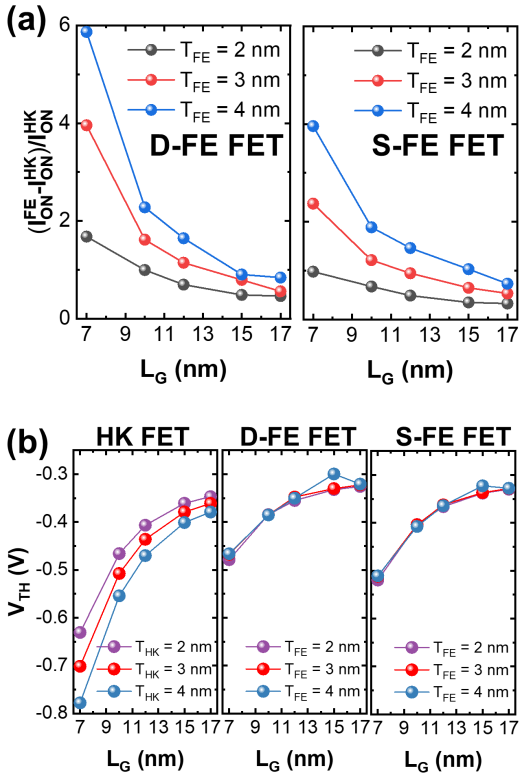

Fig. 5. (a) Relative increase in I_{ON} that is $(I_{ON}^{FE} - I_{ON}^{HK})/I_{ON}^{HK}$ where I_{ON}^{FE} and I_{ON}^{HK} are I_{ON} of FE-FETs and HK FETs, respectively. (b) V_{TH} as functions of L_G for various TFE and T_{HK}.

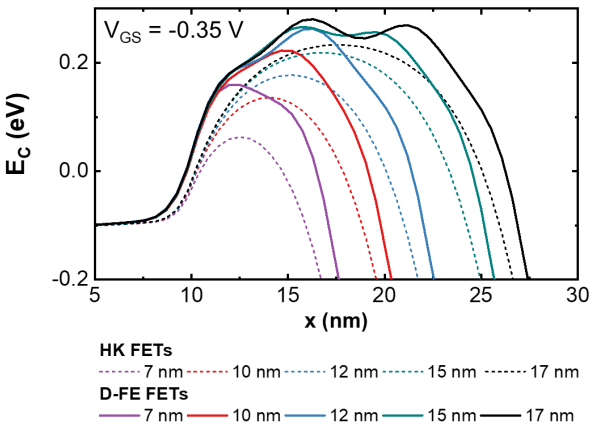

Fig. 6. Conduction band edges of HK FETs with T_{HK} = 3 nm and D-FE FETs with T_{FE} = 3 nm for various L_G at same biased condition (OFF-state for the HK FET with L_G = 17 nm and T_{FE} = 3 nm).

phase field simulations for planar FE-FETs with long L_G [4]. The performance boost is caused by the enhanced gate controllability due to the P multi-domain in FE layer. Fig. 4(a) shows the P multi-domain configuration in D-FE FETs at ON-state. Upward and downward P are alternately induced to minimize the total energy of the FE layer through the domain interaction terms. As V_{GS} increases, the domains of P whose direction points to the channel region expand and their magnitudes increase, while the domains pointing to the gate contact are reduced in width and magnitude. This is shown in Fig. 4(b), where P in the bottom FE layer is plotted for ON- and OFF-states. This makes the electric field from the P bound charges decreasing the conduction band edge (E_C) near the source-channel junction region. Thus, more electrons are injected from the source contact, increasing I_{ON}. This is clearly shown in Fig. 4(c), where E_C and the energy-resolved current density are plotted at ON-state for D-FE FETs and HK FET.

The performance boost in DG FE-FETs shows up more pronounced as L_G decreases, compared to HK FETs for same L_G. Fig. 5(a) shows the relative changes in I_{ON}, $(I_{ON}^{FE} - I_{ON}^{HK})/I_{ON}^{HK}$, where I_{ON}^{FE} and I_{ON}^{HK} are I_{ON} of FE-FETs and HK FETs, respectively. It is shown that as L_G decreases, I_{ON} of FE-FET greatly increases compared to HK FET. Also, the improvement is enhanced as the number of FE stacks increases. For HK FETs, V_{TH} rapidly decreases with L_G due to the drain-induced barrier lowering (DIBL), causing the significant degradation of I_{ON}.

For FE-FETs, DIBL is greatly reduced due to the P bound charges near the channel-drain junction. Fig. 5(b) shows V_{TH}

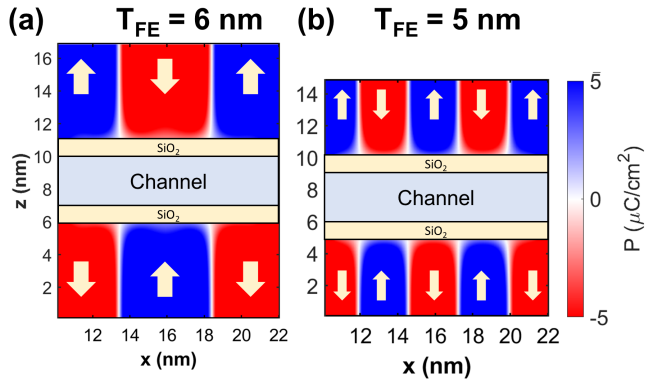

Fig. 7. P multi-domain configurations for (a) T_{FE} = 6 nm and (b) T_{FE} = 5 nm of D-FE FETs with L_G = 12 nm.

for HK FETs and FE-FETs as functions of L_G. It is shown that for FE-FETs, V_{TH} shift due to the decrease of L_G is greatly reduced compared to that of HK FETs. This is because the negative P bound charges at the drain junction reduce DIBL. This reduced DIBL is clearly seen in E_C at the same biased condition. Fig. 6 shows E_C of HK FETs and D-FE FETs for various L_G at the OFF-state of the HK FET with T_{HK} = 3 nm and L_G = 17 nm. For L_G = 17 nm, the maximum of E_C (E_C^{max}) of D-FE FET is higher than that of HK FET, due to the negative P bound charges. As L_G decreases, E_C^{max} is more raised up, and so the V_{TH} shift decreases. This is because the number of the P domains decreases with L_G, and thus the electrostatic effect of the bound charges on the channel region is enhanced. As the number of FE stacks increases, V_{TH} shift by L_G scaling down is more decreased as shown in Fig. 5(b). This is because the channel with the thickness of 3 nm is so thin that the impacts of the bound charges at the two interfaces are superimposed.

In FE-FETs, abrupt performance degradation is observed. See Fig. 3. For L_G = 12 nm, as T_{FE} increases from 5 nm to 6 nm, SS_{avg} abruptly increases and I_{ON} abruptly decreases. Note that for L_G = 7 nm, they are almost the same. The abrupt degradation is also seen for D-FE FETs, where the degradation occurs at L_G = 10 nm in addition to L_G = 12 nm, showing poorer performances than that of L_G = 7 nm.

The abrupt behavior is caused by the double barrier shaped potential profile induced by the multi-domain. Fig. 7(a) shows the P configurations at OFF-state of D-FE FET at T_{FE} = 6 nm and L_G = 12 nm. For both top and bottom FE layers, the number of P domains is 3. P near the middle of the channel is pointed towards the channel, pushing down the potential energy. At the same time, P of the side ones are pointed towards the gate contact, raising up the potential energy. The up/down/up (donw/up/down) configuration for the top (bottom) FE layer makes the channel potential profile like the double-barrier well.

For short channel devices, the multi-domain induced potential profiles cause the direct source-to-drain tunneling leakage (DSDT) current at OFF-state. Fig. 8 show the position- and

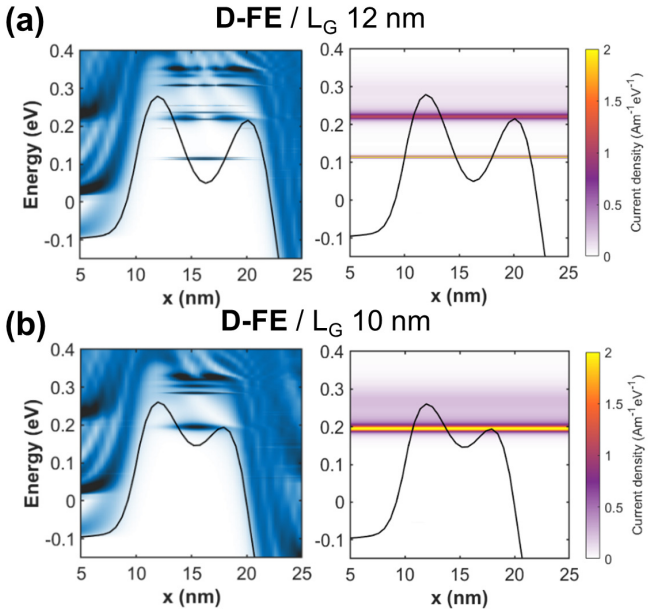

Fig. 8. Energy- and position-resolved density-of-states and current densities of D-FE FETs for (a) L_G = 12 nm and (b) L_G = 10 nm at OFF-state. Solid lines indicate the minimum of E_C. Source fermi level is set to zero.

energy-resolved density-of-states and the current densities for L_G = 10 nm and 12 nm of D-FE FETs with T_{FE} = 6 nm. The double-barrier well is seen in the figure due to the P multi-domain configuration of Fig. 7(a). The DSDT leakage through the quasi-bound states in the well greatly contributes to the OFF-state current, resulting the abrupt behavior.

The abrupt performance degradation disappears in the absence of the double-barrier well. Fig. 7(b) shows the P configuration for T_{FE} = 5 nm. Compared to the case of T_{FE} = 6 nm shown in Fig. 7(a), the number of P domains increases, reversing the P polarity near the middle of the channel. In addition, the increase in the number of the domains within the same channel length reduces the domain width, making the P bound charge effect weakened. The decrease of the double-barrier height is observed due to the decrease in the domain width in Fig. 8(b). For the two reasons, the DSDT leakage is suppressed at OFF-state, and thus the abrupt behavior disappears. This also explains the absence of the abrupt behavior for extremely scaled L_G below 10 nm.

IV. CONCLUSIONS

In this work, we investigated the short channel effects on the FE-FETs using the phase-field based quantum transport simulations. We have found that DIBL is reduced in the case of FE-FETs compared to HK FETs, due to the P bound charges effect near the drain junctions. This makes FE-FETs promising candidates for future technology nodes, replacing the HK FETs. We also found that the multi-domain induced potential profile causes the DSDT leakage current, greatly contributing to the OFF-state current and abrupt performance degradation.

ACKNOWLEDGMENT

This work was supported by Samsung Electronics Co., Ltd. (IO201218-08230-01)

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