On the Resiliency of NC-FinFET SRAMs against Variation: MFIS Structure

[1]Aniket Gupta, [1,2]Nitanshu Chauhan, [3]Om Prakash and [4]Hussam Amrouch
[1]Dept. of Electronics Engineering, National Institute of Technology (NIT) Uttarakhand, India,
[2]Dept. of Electronics and Communication Engineering, Indian Institute of Technology (IIT) Roorkee, India,
[3]Dept. of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany,
[4]Chair of Semiconductor Test and Reliability (STAR), University of Stuttgart, Germany
Email: amrouch@iti.uni-stuttgart.de

***Abstract*—This work investigates, for the first time, the impact of different variability sources on the reliability of SRAMs implemented using the Negative Capacitance FinFET (NC-FinFET) technology in comparison to the baseline conventional FinFET technology. Unlike the existing state of the art, our investigation is for NC-FinFETs constructed in a Metal–Ferroelectric–Insulator–Semiconductor (MFIS) structure. Our analysis is based on calibrated TCAD simulations in which baseline FinFETs are calibrated to reproduce Intel 14nm measurements for both I-V characteristics and variation. NC parameters were extracted by fitting the Landau model to an experimentally-measured S shaped polarization-electric field curve. Our key focus is on revealing the individual and combined impact of variability sources on the noise margins of SRAMs. We demonstrate that NC-FinFETs based SRAMs exhibit a higher immunity against variation due to the better electrostatic integrity caused by NC.**

***Index Terms*—NC-FinFET, Variability, SRAM, Reliability.**

I. Introduction

The Negative Capacitance (NC) FET is one of the very promising technologies for ultra-low power applications due to its ability to overcome the fundamental limit of Boltzmann tyranny of 60mV/decade [1], [2]. NC effect is realized under a certain capacitance matching after replacing the conventional high-κ gate dielectric with a ferroelectric (FE) layer. One profound challenge for any technology is the reliability issues associated with it [3]–[8]. In particular, the resiliency to process variation. This holds even more for NC-FET due to the additional sources of variation stemming from the new FE layer. Variations in NC-FET are attributed to the variation in the material specific Landau parameters derived from FE parameters namely the remnant polarization (P_R) and coercive field (E_C), as well as the underlying conventional transistor variations, such as random dopant fluctuation (RDF), metal work function variation (WFV), and surface roughness (T_{FE}, T_{IL} variation) (see Fig. 1).

Our Key Contribution: This work investigates the impact of the different sources of variability such as such as random dopant fluctuation (RDF), metal work function variation (WFV), and surface roughness (T_{FE}, T_{IL} variation) (Fig. 1) on SRAM reliability for 14nm NC-FinFETs constructed in a Metal-Ferro-Insulator–Semiconductor (MFIS) configuration. Using a well-calibrated TCAD setup, we study how variation impacts each of Hold Noise Margin (HNM), Read Noise Margin (RNM) and Write Noise Margin (WNM) of SRAMs.

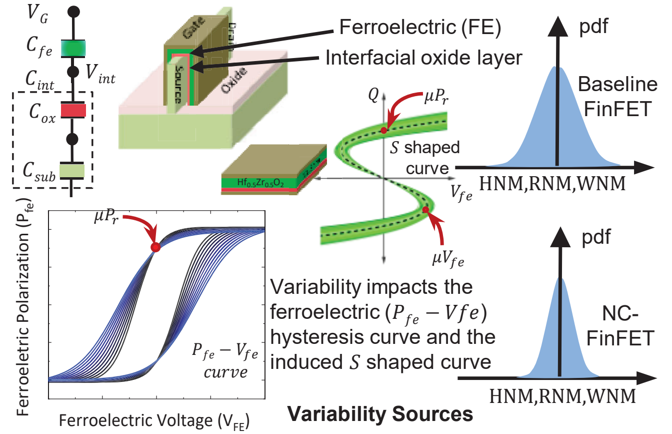
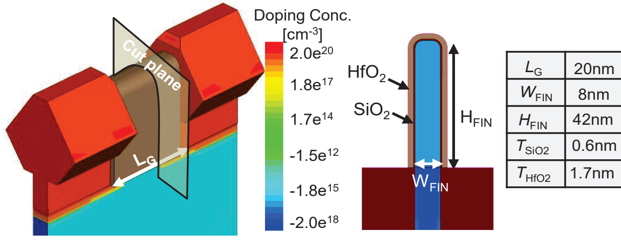


Fig. 1: Overview of our variability study for FinFET and NC-FinFET devices. In addition to considering the variability effects in the FE layer, various sources of variability (WFV, RDF, GDSR) in the underlying constituent device impact the statistical distribution of the main figures-of-merit of SRAM cells (i.e., noise margins) such as HNM, RNM and WNM.

II. TCAD Setup and Calibration for Device Simulation

Fig. 2 shows the 3D baseline FinFET schematic along with device dimensions. The simulation framework is done using Sentaurus TCAD [10]. Both n-FinFET and p-FinFET are well calibrated against measured transfer and output characteristics from reported experimental data for Intel 14nm FinFET [9]. Each of the gate metal work function, Gaussian doping profile in the source/drain (S/D) extension region, inversion and accumulation field mobility parameters along with consideration of high-κ(HfO_2)-SiO_2 interface mobility degradation, and high field saturation parameters are all carefully tuned to calibrate

978-1-6654-0685-7/21/$31.00 ©2021 IEEE



L_G	20nm
W_{FIN}	8nm
H_{FIN}	42nm
T_{SiO2}	0.6nm
T_{HfO2}	1.7nm

Fig. 2: FinFET model along with a cross section and the geometric parameters for the baseline FinFET.

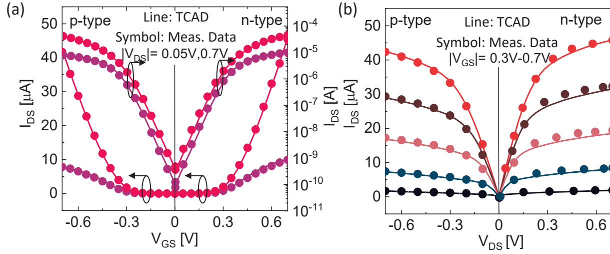


Fig. 3: (a, b) show the baseline FinFET calibration for both transfer and output characteristics demonstrating the good match between TCAD results and measurement data [9].

both n-type and p-type baseline FinFET (Fig. 3). Simulations are also comprised of Fermi–Dirac statistics with band-gap narrowing model to account for high carrier densities. To design our NC-FinFET, high-κ oxide layer of baseline devices (Fig. 2) is replaced with the FE layer of the same thickness and the rest of the physical parameters (e.g., L_g, T_{SiO2}, W_{Fin}, H_{Fin}, etc.) are kept same as the baseline FinFET. In order to include NC effect in FE layer, the Landau-Khalatnikov (L-K) equation of the electric field in FE (E_{FE}) as a function of polarization (P_{FE}), as described by Eq. 1 is coupled within baseline FinFET calibrated model.

$$E_{FE} = 2\alpha P_{FE} + 4\beta P_{FE}^3 + 4\gamma P_{FE}^5 - 2g\Delta P_{FE} + \rho(\frac{dP_{FE}}{dt}) \quad (1)$$

where α , β and γ are the Landau coefficients. The domain interaction coefficient g and the viscosity coefficient ρ in L-K equation are taken from [10]. Other FE parameters: α , β and γ are extracted by fitting the Landau model to an experimentally-measured S polarization-electric field curve [2] (Fig. 4 (a)). Including an FE layer provides a internal voltage amplification associated with the surface potential can be achieved as explained in [11]. Thus, the current *increases* and the sub-threshold slope *decreases* for both n-type and p-type NC-FinFET as shown in Fig. 4 (b).

The variability sources (RDF, WFV, GDSR, etc.) are implemented in TCAD through the impedance field method [12]–[14]. Grain probability and grain work function of the gate metal have been carefully tuned along with tuning of surface roughness of Interfacial layer and high-κ or FE layer by tuning the amplitude and resolution of geometric variation to calibrate with the Intel 14nm FinFET measurement

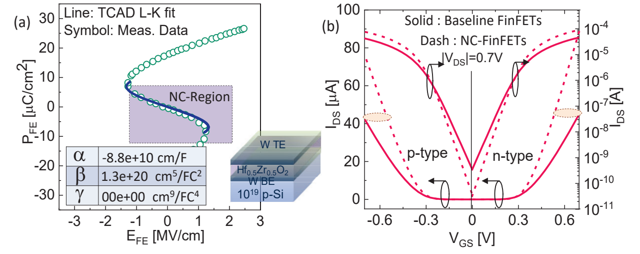


Fig. 4: (a) shows the fitted S curve for the FE CAP based on the L-K parameters obtained from [2]. (b) Impact of replacing the high-κ HfO2 in the baseline FinFET with an FE layer to realize NC effect demonstrating the improvements in the drain current (I_{DS}) as compared to baseline FinFETs.

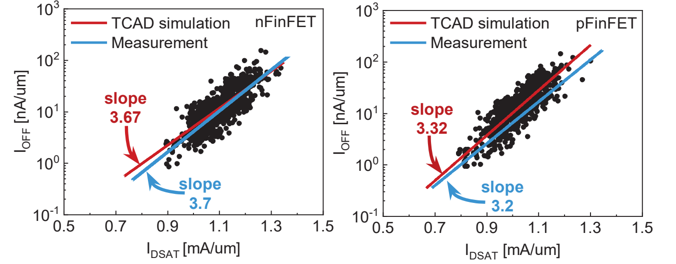
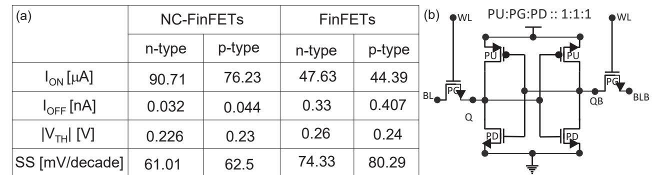


Fig. 5: I_{OFF} vs. I_{DSAT} variability data obtained from TCAD simulations are benched marked against the variability measurement data from Intel 14 nm FinFETs [9] for both baseline nFinFET and pFinFET devices respectively.

variability data available in [9] (Fig. 5). However due to additional steps involved in the fabrication of NC-FinFET due deposition of ferroelectric layer (e.g., zirconium doped HfO2) as compared to baseline FinFET. In order to account for this additional source of variability in case of NC-FinFET, we have additionally included Ferroelectric Variability (FEV) which is not readily supported in TCAD. To consider variation in NC-FinFET (i.e., in the material specific L-K parameters (α, β) for NC), we employ Monte-Carlo simulations with σ/μ = 5% variation in FE parameters (P_r, E_c) to account for the process variation. Then, the worst case (i.e., boundary condition) is extracted. Note that with respect to NC effect, such a worst case occurs when P_r increases and E_c decreases. Finally, TCAD mixed-mode simulations are performed for



(a)	NC-FinFETs		FinFETs	
	n-type	p-type	n-type	p-type
I_{ON} [µA]	90.71	76.23	47.63	44.39
I_{OFF} [nA]	0.032	0.044	0.33	0.407
$\lvert V_{TH} \rvert$ [V]	0.226	0.23	0.26	0.24
SS [mV/decade]	61.01	62.5	74.33	80.29

Fig. 6: (a) shows the key electrical characteristics of n-type and p-type transistors in NC-FinFET and its counterpart baseline FinFET. (b) Schematic of the used 6-T SRAM cell.

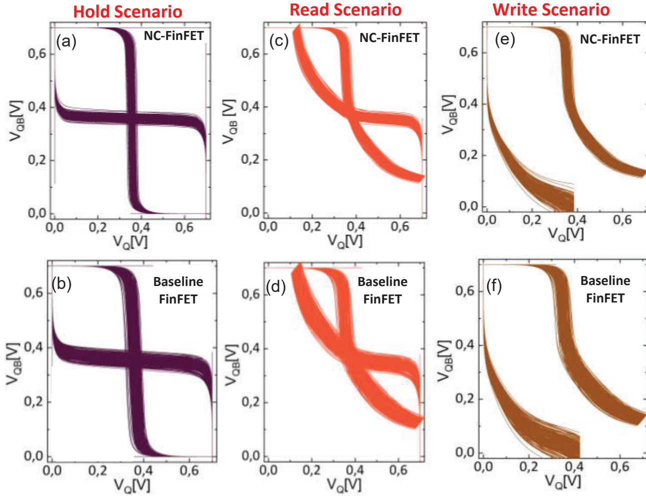


Fig. 7: (a-f) Butterfly curves comparisons between NC-nFinFET SRAMs and their counterpart baseline FinFET SRAMs under the combined impact of all variability sources. Three different scenarios of SNMs are analyzed and compared.

a compete 6-T SRAM (Fig. 6) under the variability effects (both individual and combined impact of sources) towards comparing various noise margins in the baseline FinFET SRAMs and their counterpart NC-FinFET SRAMs.

III. Results and Discussion

A. Impact of Variability on Butterfly Curves of SRAMs

In Fig. 7 (a-f), we present the comparisons between butterfly curve of NC-FinFETs based SRAM and their counterpart baseline FinFETs based SRAM under the combined impact of all variability sources. Three scenarios are investigated: (1) Hold Noise Margin (see Fig. 7 (a, b)), (2) Read Noise Margin (see Fig. 7 (c, d)), and (3) Write Noise Margin (see Fig. 7 (e, f)). Note that NC-FinFET SRAMs are subject to FE variation (FEV) besides the other variability sources that originally impact the baseline FinFET SRAMs. As shown in Fig. 7(a-f), NC-FinFET based SRAMs can accommodate larger fitted square compared to baseline SRAMs due to sharper transition in the Voltage Transfer Characteristic (VTC) arising from the reduced sub-threshold swing (SS) in case of NC-FinFET devices. This, in turn, results in a better Static Noise Margin (SNM) for all three scenarios (i.e., HNM, RNM, and WNM) [15]. Furthermore, NC-FinFET based SRAMs exhibit smaller variations, which can be attributed to the lesser variation in their NC-nFinFET and NC-pFinFET devices obtained from the better electrostatic integrity of the gate over the channel caused by the NC effect (see Fig. 6 (a)).

B. Impact of Variability on Static Noise Margins (SNMs)

In Fig. 8 (a, b), we demonstrate the distributions of HNM, similarly Fig. 8 (d, e) demonstrate the distributions for RNM and Fig. 8 (g, h) demonstrate the distributions of WNM for both NC-FinFET SRAMs and its counterpart baseline

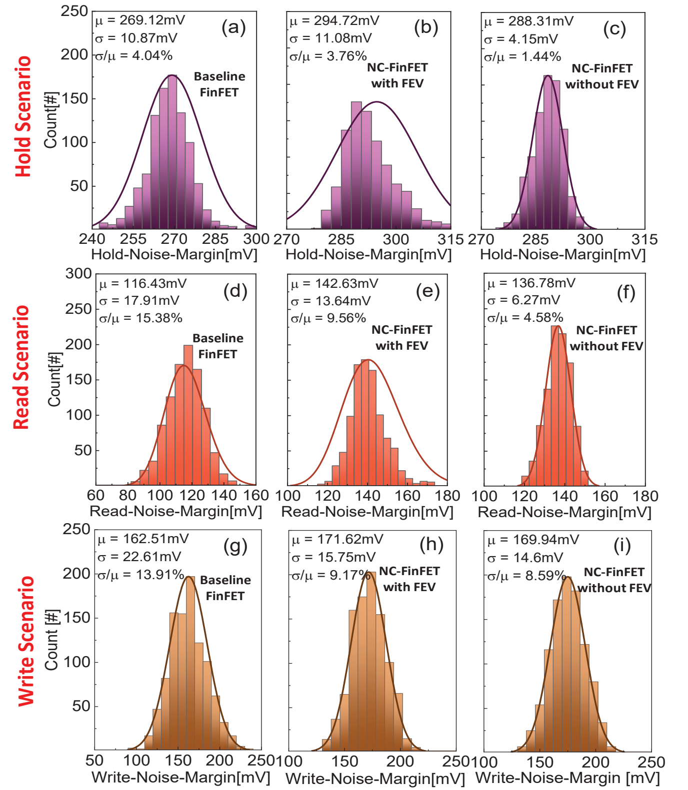


Fig. 8: (a-i) Impact of variability on the SNMs comparing NC-FinFET SRAMs and baseline FinFET SRAMs. (a-c) Hold Noise Margin (HNM). (d-f) Read Noise Margin (RNM). (g-i) Write Noise Margin (WNM).

FinFET SRAMs under the combined impact of all variability sources. NC-FinFET SRAMs have a larger mean value (μ) of SNM as well as a smaller variation (σ/μ) compared to their counterpart FinFET SRAMs in all three scenarios (HNM, RNM and WNM). As shown in the Figures, in case of NC-FinFET based SRAMs the mean value of HNM increases from 269.12mV to 294.72mV and reduces σ/μ from 4.04% to 3.76%. Similarly, the mean value for RNM increases from 116.43mV to 142.63mV and considerably reduces σ/μ from 15.38% to 9.56% and the mean value of WNM increases from 162.51mV to 171.62mV and reduces σ/μ from 13.91% to 9.17%. As a result, NC-FinFET SRAMs have a higher resiliency to noise in all three scenarios due to the larger mean SNM (μ) and smaller susceptibility to variation (σ/μ %).

C. Impact of Ferroelectric Variation on NC-FinFET SRAMs

To better understand the degradation induced by the FE variation (FEV) itself, we additionally present in Fig. 8 comparisons between the HNM, RNM and WNM distributions in the presence and absence of FE variation, i.e., with and without FEV. As can be noticed, FEV diminishes to some degree the obtained gain from NC effect and hence NC-FinFET SRAMs suffer more from variations. As shown, FEV increases the overall variation (σ/μ %). For the HNM scenario, the

σ/μ variation increases from 1.44% to 3.76%. Similarly, for RNM and WNM scenarios, σ/μ variation also increases; from 4.58% to 9.56% and from 8.59% to 9.17%, respectively. This demonstrates the critical role that variation in the ferroelectric layer plays in the resiliency of SRAMs to noise.

D. Impact of Individual Variability Sources on SRAMs

Finally, we decompose in Fig. 9, the overall standard deviation (σ) in the static noise margins of SRAM (i.e., HNM, RNM, and WNM) into the individual sources to demonstrate the impact of each of WFV, RDF, and GDSR variation standalone. In all three scenarios (i.e., Hold, Read and Write operation), the variation is dominant by the RDF and WFV effects. NC noticeably reduces WVF and RDF induced variation in all three scenarios and helps in mitigating the deleterious impact of RDF and WFV.

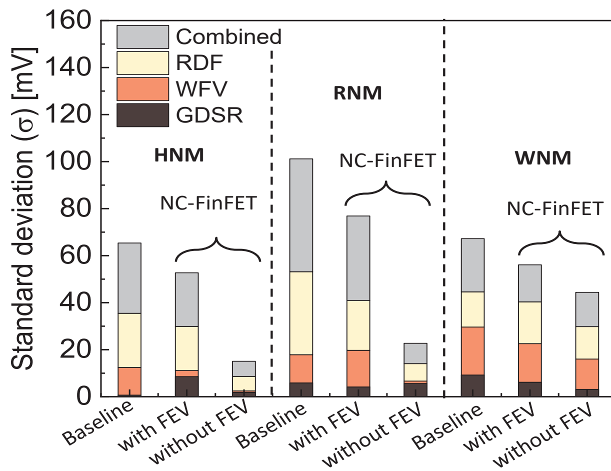


Fig. 9: Impact of individual variability sources on HNM, RNM and WNM variations comparing NC-FinFET SRAMs and baseline FinFET SRAMs.

IV. Conclusion

The impact of different variability sources on both FinFET and NC-FinFET based SRAM is investigated through extensive mixed-mode TCAD simulations. Our result shows that the hold, read, and write noise margins of 6-T SRAM have better resiliency against variation compared to the baseline FinFET due to the better electrostatic integrity caused by the internal voltage amplification provided by the FE layer.

Acknowledgment

Authors would like to thank Simon Thomann from KIT and Govind Bajpai for their help in SRAM variability analysis. Authors are grateful to Girish Pahwa from the University of California, Berkeley and Yogesh Chauhan from IIT Kanpur for their valuable discussions and support in NCFET.

This work was supported in part by the Office of Naval Research under Grant N00014-18-1-2672.

References

[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters*, vol. 8, no. 2, pp. 405–410, 2008, pMID: 18052402. [Online]. Available: https://doi.org/10.1021/nl071804g

[2] M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, "Demonstration of high-speed hysteresis-free negative capacitance in ferroelectric hf0.5zr0.5o2," in *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018, pp. 31.6.1–31.6.4. [Online]. Available: https://doi.org/10.1109/IEDM.2018.8614677

[3] G. Bajpai, A. Gupta, O. Prakash, G. Pahwa, J. Henkel, Y. S. Chauhan, and H. Amrouch, "Impact of radiation on negative capacitance finfet," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, pp. 1–5. [Online]. Available: https://doi.org/10.1109/IRPS45951.2020.9129165

[4] O. Prakash, A. Gupta, G. Pahwa, J. Henkel, Y. S. Chauhan, and H. Amrouch, "Impact of interface traps on negative capacitance transistor: Device and circuit reliability," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 1193–1201, 2020. [Online]. Available: https://doi.org/10.1109/JEDS.2020.3022180

[5] A. Gupta, G. Bajpai, P. Singhal, N. Bagga, O. Prakash, S. Banchhor, H. Amrouch, and N. Chauhan, "Traps based reliability barrier on performance and revealing early ageing in negative capacitance fet," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021, pp. 1–6. [Online]. Available: https://doi.org/10.1109/IRPS46558.2021.9405185

[6] G. Bajpai, A. Gupta, O. Prakash, Y. S. Chauhan, and H. Amrouch, "Soft errors in negative capacitance fdsoi srams," in *2021 5th IEEE Electron Devices Technology Manufacturing Conference (EDTM)*, 2021, pp. 1–3. [Online]. Available: https://doi.org/10.1109/EDTM50988.2021.9421043

[7] O. Prakash, A. Gupta, G. Pahwa, J. Henkel, Y. S. Chauhan, and H. Amrouch, "Impact of interface traps induced degradation on negative capacitance finfet," in *2020 4th IEEE Electron Devices Technology Manufacturing Conference (EDTM)*, 2020, pp. 1–4. [Online]. Available: https://doi.org/10.1109/EDTM47692.2020.9118008

[8] H. Amrouch, G. Pahwa, A. D. Gaidhane, C. K. Dabhi, F. Klemme, O. Prakash, and Y. S. Chauhan, "Impact of variability on processor performance in negative capacitance finfet technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3127–3137, 2020.

[9] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu *et al.*, "A 14nm logic technology featuring 2 nd-generation finfet, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm 2 sram cell size," in *2014 IEEE International Electron Devices Meeting*. IEEE, Dec 2014, pp. 3–7, doi:10.1109/IEDM.2014.7046976.

[10] "Sentaurus device user guide, version p-2019.03-sp1, synopsys, inc. mountain view, ca, usa." Accessed: April, 2020. [Online]. Available: https://www.synopsys.com/

[11] J. Jo, A. I. Khan, K. Cho, S. Oh, S. Salahuddin, and C. Shin, "Capacitance matching effects in negative capacitance field effect transistor," in *2016 IEEE Silicon Nanoelectronics Workshop (SNW)*, 2016, pp. 174–175. [Online]. Available: https://doi.org/10.1109/SNW.2016.7578038

[12] K. El Sayed, E. Lyumkis, and A. Wettstein, "Modeling statistical variability with the impedance field method," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, 2012, pp. 205–208. [Online]. Available: http://in4.iue.tuwien.ac.at/pdfs/sispad2012/11-2.pdf

[13] F. Bonani, G. Ghione, M. Pinto, and R. Smith, "An efficient approach to noise analysis through multidimensional physics-based models," *IEEE Transactions on Electron Devices*, vol. 45, no. 1, pp. 261–269, 1998. [Online]. Available: https://doi.org/10.1109/16.658840

[14] A. Wettstein, O. Penzin, E. Lyumkis, and W. Fichtner, "Random dopant fluctuation modelling with the impedance field method," in *International Conference on Simulation of Semiconductor Processes and Devices, 2003. SISPAD 2003.*, 2003, pp. 91–94. [Online]. Available: https://doi.org/10.1109/SISPAD.2003.1233645

[15] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of process variations on negative capacitance finfet devices and circuits," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147–150, 2018. [Online]. Available: https://doi.org/10.1109/LED.2017.2770158