Negative-Capacitance FETs for Advanced Nodes: Circuit Performance and Variability Analysis with Ferroelectric Dynamic Switching

Yen-Kai Lin[1,*], Jing Wang[1], Takeshi Okagaki[2], Seonghoon Jin[1], Anh-Tuan Pham[1],
Yonghee Park[2], Uihui Kwon[2], Woosung Choi[1], and Dae Sin Kim[2]
[1]Device Lab, DSA R&D, Samsung Semiconductor, Inc., San Jose, CA, USA. [*]Email: yen-kai.lin@samsung.com
[2]Data & Information Technology Center, Samsung Electronics, Hwasung-si Gyeonggi-do, South Korea.

***Abstract*—In this paper, circuit benchmark of negative capacitance FinFET (NC-FinFET) are conducted using the in-house TCAD based on 7-nm and 14-nm FinFET technologies with high-κ dielectric replaced by ferroelectric material. The compact model is calibrated accordingly for circuit simulations. Compared with reference FinFET, NC-FinFET enables I_{OFF} reduction and DIBL/SS/I_{ON} enhancements. The results of ring oscillator (RO) analysis using the calibrated compact model suggest that 1) the ferroelectric (FE) dipole switching dynamics has negligible impact on the RO delay with the reported FE parameters, and 2) the NC-FinFET-based RO enables energy saving via V_{DD} scaling at a fixed propagation delay. Finally, the impact of FE variability on transistor and circuit metrics is analyzed and found to be insignificant compared to other FinFET variation sources**

Keywords—compact modeling; process variations; negative-capacitance FET (NCFET); circuit; ferroelectrics

I. Introduction

NC-FinFET is a CMOS technology-compatible device, featuring steeper SS and improved I_{ON} [1, 2], thereby the performance of circuits consisting of NC-FinFETs using the state-of-the-art FinFET technology is attractive. Although the controversial question about the intrinsic limit of ferroelectric dipole response was clarified [3, 4], the more systematic comparison on FinFET- and NC-FinFET-based ring oscillators (ROs) is required based on the state-of-the-art technology. There are some literatures discussing NC-FinFET circuit metrics [5−8]. However, the performance could be overestimated due to the uncalibrated capacitances and the presence of internal metal which theoretically eliminates hysteresis-free operation [9, 10]. Furthermore, the doping-relied ferroelectric (FE) may also suffer from properties variations [11] and impact the variability in devices and circuits.

In this paper, we addressed the above questions by utilizing the TCAD simulations based on the advanced FinFET technology nodes and the calibrated compact models for circuit simulations, assuming that the FE can be properly integrated into those technologies. The results indicated the negligible impact of FE switching dynamics and FE property variations on devices and circuits.

II. Device Calibration and Simulation Methodology

The in-house TCAD is first calibrated with 7-nm and 14-nm FinFET technologies (V_{DD} = 0.75 and 0.8 V) for both I_{DS}−V_{GS} and C_{GG}−V_{GS}, as shown in Fig. 1, with the FinFET geometry and electrical targets from the PDKs. The NC-FinFET performances of P_r = 10 μC/cm^2 and E_C = 1 MV/cm (Fig. 2) are predicted by the TCAD which internally solving the Poisson and Landau-Khalatnikov equations self-consistently with only converting the high-κ dielectric to FE ($t_{high\text{-}\kappa} = t_{FE}$) by employing doping [12]:

$$V_{FE} = t_{FE}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

where α, β, and γ are the ferroelectric material parameters which can be related to P_r and E_C [7]. For HfO_2-based FE (γ = 0) assumed in this study, $\alpha = (-3\sqrt{3}/4) \cdot (E_C/P_r)$ and $\beta = (3\sqrt{3}/8) \cdot (E_C/P_r^3)$.

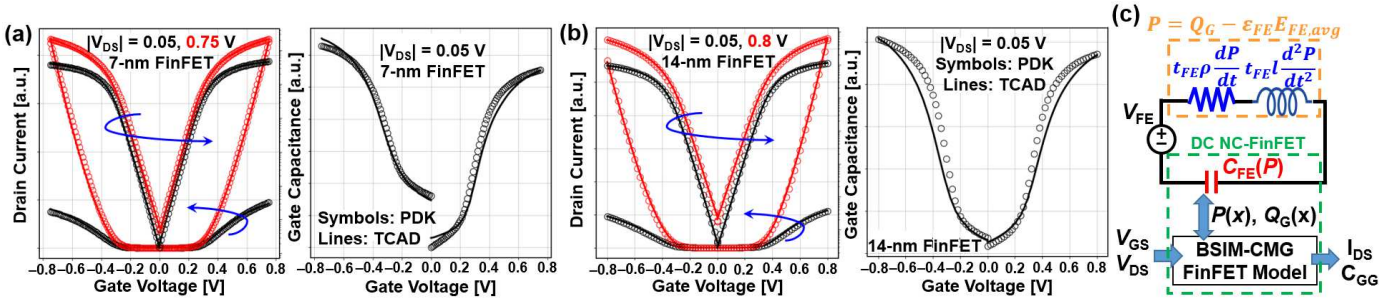

Fig. 1: TCAD calibrations for (a) 7-nm and (b) 14-nm FinFETs (Symbols: PDK; lines: TCAD). (c) RLC sub-circuit model for FE dipole dynamic switching [3] coupled with DC NC-FinFET model. $E_{FE,avg}$ is the average of electric field at source and drain sides, and ε_{FE} (= 16) is the permittivity.

978-1-6654-0685-7/21/$31.00 ©2021 IEEE

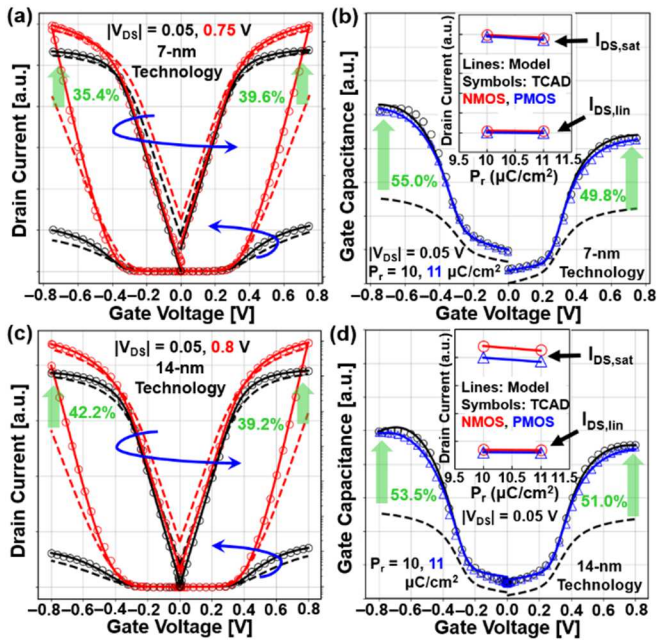

Fig. 2: NC-FinFET compact model (solid) vs. TCAD (symbols) for 7-nm/14-nm technologies: (a)/(c) I_{DS}–V_{GS} and (b)/(d) C_{GG}–V_{GS}. [FinFET data (dashed) generated from PDK are included for comparison.] The insets of (b) and (d) show the predictive nature of compact model for a 10% P_r change.

TABLE I
EXPERIMENTAL FERROELECTRIC DYNAMICS PARAMETERS

Method	Optical [3]	Electrical [15]	
		X-parameter	S-parameter
ρ (Ω·m)	0.0018	0.0022	0.00193
l (H·m)	50×10^{-18}	N/A	N/A

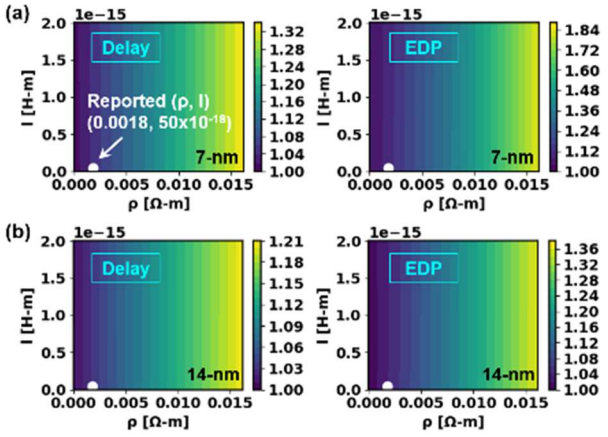

Fig. 3: Impact of ρ and l on normalized delay and EDP of (a) 7-nm and (b) 14-nm ring oscillators [C_{load} = 1f (F)], showing l term is negligible. Only small penalty on delay and EDP is observed with reported ρ and l values [3].

The BSIM-CMG-based NC-FinFET compact model [13, 14], which spatially solves the electrostatics with Landau-Khalatnikov equations (a distributed model), was calibrated with the mentioned TCAD data (Fig. 2). The FE dynamic

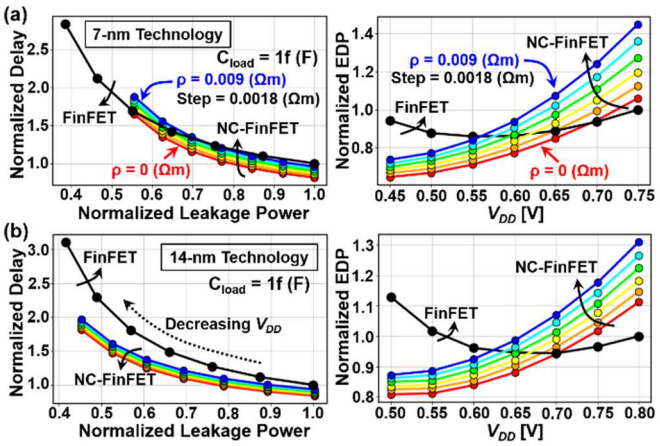

Fig. 4: Normalized delay and EDP of (a) 7-nm and (b) 14-nm ring oscillators with $l = 50 \times 10^{-18}$ (H·m), and various ρ with C_{load} = 1f (F).

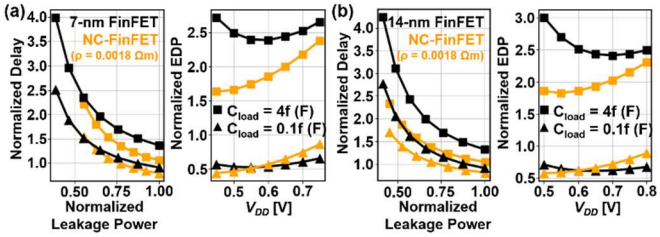

Fig. 5: Normalized [to C_{load} = 1f (F) case] delay and EDP of (a) 7-nm and (b) 14-nm ring oscillators with $l = 50 \times 10^{-18}$ (H·m) and ρ = 0.0018 (Ω·m) with C_{load} = 0.1f (F) and 4f (F).

switching is modeled by an RLC sub-circuit with the viscosity parameter ρ (the first order dP/dt term) and the kinetic inductance parameter l (the second order d^2P/dt^2 term) [3], as shown in Fig. 1 (c). The experimentally measured values of ρ and l by optical [3] and electrical measurement [15] are listed in Table I. The circuit performance is evaluated using a 7-stage FO4 ring oscillator with 10 fins for each transistor, and the impact of the load capacitance will be examined. The calibrated compact model is predictive for FE properties with only varying FE parameters by 10% (Fig. 2), which ensures the accuracy of variability modeling. The 7-nm and 14-nm FinFET PDKs enable the statistical global variations combined with the additional FE property variations in NC-FinFET, and thereby variability in ROs. Note that the threshold voltage (V_{TH}) of NC-FinFET is shifted to match the I_{OFF} of reference FinFET for fair comparison of circuit performance metrics.

III. RESULTS AND DISCUSSION

A. Ring Oscillator Analysis

Fig. 3 shows the impact of the FE dynamic switching parameters ρ and l on the delay (τ) and energy-delay-product (EDP = $I_{DDA}V_{DD}\tau^2$) of ROs for 7-nm and 14-nm NC-FinFETs. The second-order term is negligible as long as the oscillation frequency is << 10 THz [3, 15], which is much below frequency range of interest in this study. It is observed that there is only little delay and EDP penalty with the reported

TABLE II
SUMMARY OF RING OSCILLATOR PERFORMANCE OF NC-FINFET COMPARED WITH FINFET UNDER ISO-DELAY CONDITION

	7-nm Technology		14-nm Technology	
V_{DD} [V]	0.75→**0.63**	0.75→**0.59**	0.8→**0.7**	0.8→**0.66**
C_{load} [F]	1f	4f	1f	4f
C_{eff}	20.1%↑	8.8%↑	25.2%↑	12.2%↑
R_{eff}	16.4%↓	6.6%↓	19.7%↓	9.3%↓
Energy	15.2%↓	32.7%↓	4.1%↓	23.7%↓

ρ = 0.0018 (Ω·m) and l = 50 × 10^{-18} (H·m).

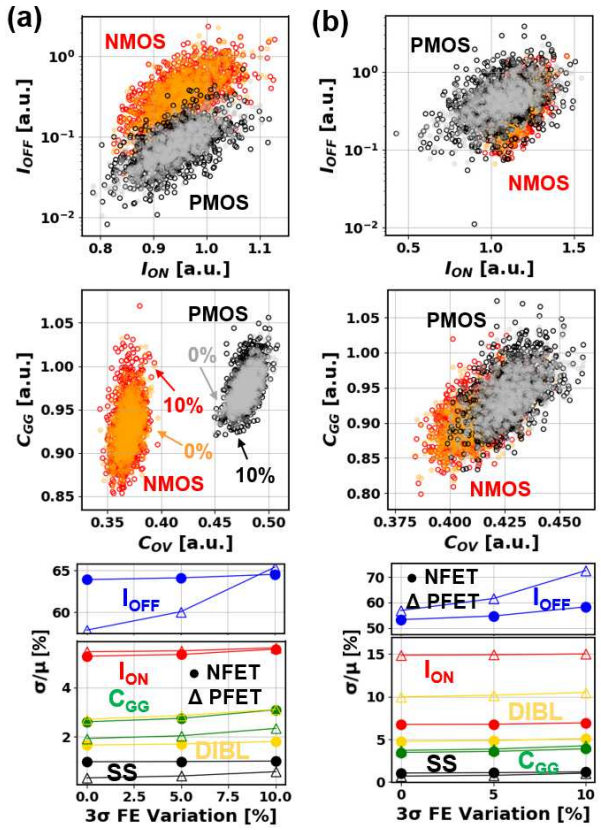

Fig. 6. Scatter plots and coefficient of variation of I_{OFF}, I_{ON}, C_{OV}, C_{GG}, SS, and DIBL of (a) 7-nm and (b) 14-nm NC-FinFETs with 3σ FE variations of 0% and 10% (1000 samples). Note that the FE thickness variation is assumed the same as HfO_2 variation in FinFET technology.

values of ρ = 0.0018 (Ω·m) and l = 50 × 10^{-18} (H·m) [3] as denoted by white dots in Fig. 3.

Fig. 4 (a) and (b) show the delay versus leakage power and EDP versus V_{DD} curves of 7-stage FO4 ROs consisting of the 7-nm/14-nm FinFETs and NC-FinFETs. The strong effect of ρ term is observed (also see Fig. 3) but fortunately a small ρ is experimentally reported based on optical and electrical measurements [3, 15]. Under the iso-delay condition, the V_{DD} of 14-nm NC-FinFET-based RO with ρ = 0.0018 (Ω·m) and l = 50 × 10^{-18} (H·m) can be scaled from 0.8 V down to 0.7 V to achieve a 4.1% energy reduction with C_{load} = 1f (F) ~ $C_{GG,FinFET}$ with 10 fins (intermediate load). More energy saving of 15.2% is observed in the 7-nm case where the V_{DD} of NC-FinFET can be scaled from 0.75 V down to 0.63 V. Although there is a penalty on C_{eff} [= EDP/($V_{DD}^2\tau$)] of NC-FinFET, the compensation of better R_{eff} (= τ/C_{eff}) leads to scaled V_{DD} and thus energy-efficiency. At high load of C_{load} = 4f (F), the energy saving of 7-nm/14-nm NC-FinFET is even more significant (32.7%/23.7%) with the further scaled V_{DD} = 0.59 V/0.66 V because of higher drive current of NC-FinFETs [see Fig. 5 (a) and (b)] to charge/discharge the parasitic capacitance. The results are summarized in Table II. However, C_{load} = 0.1f (F) (low load) leads to energy inefficiency due to NC-enhanced gate capacitance of NC-FinFET (Fig. 2). For 7-nm/14-nm NC-FinFET with low load, scaling V_{DD} from 0.75 V/0.8 V to 0.65 V/0.7 V under iso-delay leads to the similar energy and 6% more energy consumptions, respectively.

TABLE III
SUMMARY OF COEFFICIENT OF VARIATION OF DELAY AND ENERGY WITH 3σ FERROELECTRIC PROPERTIES VARIATIONS

3σ [%]	7-nm Technology: V_{DD} = 0.63, 0.59 [V], C_{load} = 1f, 4f [F]		14-nm Technology: V_{DD} = 0.70, 0.66 [V], C_{load} = 1f, 4f [F]	
	σ/μ [%]			
	Delay	Energy	Delay	Energy
0	5.43, 6.35	2.64, 1.16	9.07, 9.27	2.24, 1.26
5	5.48, 6.42	2.68, 1.18	9.09, 9.29	2.25, 1.26
10	5.53, 6.48	2.69, 1.23	9.12, 9.33	2.28, 1.27
15	5.57, 6.54	2.69, 1.24	9.20, 9.40	2.36, 1.30
20	5.62, 6.60	2.69, 1.26	9.58, 9.78	2.45, 1.41

ρ = 0.0018 (Ω·m) and l = 50 × 10^{-18} (H·m). The former and latter values of delay and energy in table are for different V_{DD} and C_{load} combinations.

B. NC-FinFET Variability

The variance in ferroelectric properties P_r and E_C are inevitable due to doping and strain variances [11]. Fig. 6 shows statistics of I_{OFF}, I_{ON}, C_{OV}, C_{GG}, SS, and DIBL with P_r and E_C variation of 3σ = 0%, 5%, and 10% combined with the FinFET statistical global process variations for 7-nm/14-nm technologies. The FE thickness variation is considered the same as high-κ dielectric variation due to the similar atomic layer deposition (ALD) process [16, 17] with other process modules being fixed. The I_{OFF} of NC-FinFETs are relatively sensitive to the FE variation due to the inner fringing-induced change in V_{TH} [14] and thus exponential impact on I_{OFF}. Since the SS and DIBL for the nominal NC-FinFET are low enough to 60 mV/dec and < 5 mV respectively, the FE variation does not impact the SS and DIBL much. As long as the 3σ variation of FE is less than 25% suggested in [11], the FE variations in other device metrics of both technologies are insignificant, showing the greater impact of FinFET inherent variations from PDK. Thus, it is expected that FE variations in general do not influence the RO delay and energy with a reasonably controlled ALD process and integration for FE as summarized in Table III.

IV. CONCLUSION

Although the process integration of NC-FinFET into the state-of-the-art technology requires more engineering effort, the preliminary circuit performance evaluation is demanded.

The analysis of NC-FinFET-based ring oscillators shows that the ferroelectric dynamic switching effect is negligible with the experimentally measured parameters and the NC-FinFET enables energy saving by reducing V_{DD} without any delay penalty for advanced technology nodes due to its superior drive current. Furthermore, coupled with the FinFET variation from PDK, the FE variability may not have a great impact on the ring oscillator performance. However, further experimental study on FE process integration and its impact on NC-FinFET is an important topic for future work.

REFERENCES

[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett*., vol. 8, no. 2, pp. 405–410, Feb. 2008. doi: 10.1021/nl071804g.

[2] Z. Krivokapic *et al*., "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEDM Tech. Dig.*, Dec. 2017, pp. 357–360. doi: 10.1109/iedm.2017.8268393.

[3] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEEE Electron Device Lett*., vol. 38, no. 9, pp. 1328–1330, Sep. 2017. doi: 10.1109/led.2017.2731343.

[4] D. Kwon, Y.-H. Liao, Y.-K. Lin, J. P. Duarte, K. Chatterjee, A. J. Tan, A. K. Yadav, C. Hu, Z. Krivokapic, and S. Salahuddin, "Response speed of negative capacitance FinFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 49–50. doi: 10.1109/VLSIT.2018.8510626.

[5] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-delay tradeoffs in negative capacitance FinFET based CMOS circuits," in *International Conference on Emerging Electronics (ICEE)*, Dec. 2016. doi: 10.1109/ICEmElec.2016.8074416.

[6] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of process variations on negative capacitance FinFET devices and circuits," *IEEE Electron Device Lett*., vol. 39, no. 1, pp. 147–150, Jan. 2018. doi: 10.1109/LED.2017.2770158.

[7] S. Pentapati, R. Perumal, S. Khandelwal, M. Hoffmann, S. K. Lim, and A. I. Khan, "Cross-domain optimization of ferroelectric parameters for negative capacitance transistors—Part I: constant supply voltage," *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 365–370, Jan. 2020. doi: 10.1109/TED.2019.2955018.

[8] C.-S. Hsu, C. Pan, and A. Naeemi, "Performance analysis and enhancement of negative capacitance logic devices based on internally resistive ferroelectrics," *IEEE Electron Device Lett*., vol. 39, no. 5, pp. 765–768, May 2018. doi: 10.1109/LED.2018.2820118.

[9] M. Hoffmann, M. Peši´c, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10891–10899, May 2018. doi: 10.1039/C8NR02752H.

[10] T. Rollo, F. Blanchini, G. Giordano, R. Specogna, D. Esseni, "Revised analysis of negative capacitance in ferroelectric-insulator capacitors: analytical and numerical results, physical insight, comparison to experiments," in *IEDM Tech. Dig.*, Dec. 2019, pp. 142–145. doi: 10.1109/IEDM19573.2019.8993436.

[11] Y.-K. Lin, M.-Y. Kao, H. Agarwal, Y.-H. Liao, P. Kushwaha, K. Chatterjee, J. P. Duarte, H.-L. Chang, S. Salahuddin, and C. Hu, "Effect of polycrystallinity and presence of dielectric phases on NC-FinFET variability," in *IEDM Tech. Dig.*, Dec. 2018, pp. 209–212, doi: 10.1109/iedm.2018.8614704.

[12] M. H. Park, Y. H. Lee, H. J. Kim, Y. J. Kim, T. Moon, K. D. Kim, J. Müller, A. Kersch, U. Schroeder, T. Mikolajick, and C. S. Hwang, "Ferroelectricity and antiferroelectricity of doped thin HfO2-based films," *Adv. Mater*., vol. 27, no. 11, pp. 1811–1831, Mar. 2015. doi: 10.1002/adma.201404531.

[13] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y.-K. Lin, H.-L. Chang, S. Salahuddin, and C. Hu, "Compact models of negative-capacitance FinFETs: Lumped and distributed charge models," in *IEDM Tech. Dig.*, Dec. 2016, pp. 754–757. doi: 10.1109/IEDM.2016.7838514.

[14] Y.-K Lin, H. Agarwal, P. Kushwaha, M.-Y. Kao, Y.-H. Liao, K. Chatterjee, S. Sayeef, and C. Hu, "Analysis and modeling of inner fringing field fffect on negative capacitance FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2023–2027, Apr. 2019. doi: 10.1109/TED.2019.2899810.

[15] Z. C. Yuan, P. S. Gudem, M. Wong, J. K. Wang, T. B. Hook, P. Solomon, D. Kienle, and M. Vaidyanathan, "Toward microwave S- and X-parameter approaches for the characterization of ferroelectrics for applications in FeFETs and NCFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2028–2035, Apr. 2019. doi: 10.1109/TED.2019.2901668.

[16] D. Kwon, S. Cheema, Y.-K. Lin, Y.-H. Liao, K. Chatterjee, A. J. Tan, C. Hu, and S. Sayeef, "Near threshold capacitance matching in a negative capacitance FET with 1 nm effective oxide thickness gate stack," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 179–182, Jan. 2020. doi: 10.1109/LED.2019.2951705.

[17] S. Cheema, N. Shanker, L.-C. Wang, C.-H. Hsu, S.-L. Hsu, Y.-H. Liao, M. S. Jose, J. Gomez, W. Li, J.-H. Bae, S. Volkman, D. Kwon, Y. Rho, G. Pinelli, R. Rastogi, D. Pipitone, C. Stull, M. Cook, B. Tyrrell, V. Stoica, Z. Zhang, J. Freeland, C. Tassone, A. Mehta, G. Soheli, D. Thompson, D. I. Suh, W.-T. Koo, K.-J. Nam, D. J. Jung, W.-B. Song, C.-H. Lin, S. Nam, J. Heo, C. Grigoropoulos, P. Shafer, P. Fay, R. Ramesh, J. Ciston, S. Datta, M. Mohamed, C. Hu, and S. Salahuddin, "Atomic-scale ferroic HfO_2-ZrO_2 superlattice gate stack for advanced transistors," *Naure* (in review), 2021. doi: 10.21203/rs.3.rs-413053/v1