Negative-Capacitance FETs for Advanced Nodes: 
Circuit Performance and Variability Analysis with 
Ferroelectric Dynamic Switching 

Yen-Kai Lin1,*, Jing Wang1, Takeshi Okagaki2, Seonghoon Jin1, Anh-Tuan Pham1, 
Yonghee Park2, Uihui Kwon2, Woosung Choi1, and Dae Sin Kim2

1Device Lab, DSA R&D, Samsung Semiconductor, Inc., San Jose, CA, USA. *Email: yen-kai.lin@samsung.com 
2Data & Information Technology Center, Samsung Electronics, Hwasung-si Gyeonggi-do, South Korea.

Abstract—In this paper, circuit benchmark of negative capacitance FinFET (NC-FinFET) are conducted using the in-house TCAD based on 7-nm and 14-nm FinFET technologies with high-κ dielectric replaced by ferroelectric material. The compact model is calibrated accordingly for circuit simulations. Compared with reference FinFET, NC-FinFET enables $I_{OFF}$ reduction and DIBL/SS/$I_{ON}$ enhancements. The results of ring oscillator (RO) analysis using the calibrated compact model suggest that 1) the ferroelectric (FE) dipole switching dynamics has negligible impact on the RO delay with the reported FE parameters, and 2) the NC-FinFET-based RO enables energy saving via $V_{DD}$ scaling at a fixed propagation delay. Finally, the impact of FE variability on transistor and circuit metrics is analyzed and found to be insignificant compared to other FinFET variation sources.

Keywords—compact modeling; process variations; negative-capacitance FET (NCFET); circuit; ferroelectrics

I. INTRODUCTION
NC-FinFET is a CMOS technology-compatible device, featuring steeper SS and improved $I_{ON}$ [1, 2], thereby the performance of circuits consisting of NC-FinFETs using the state-of-the-art FinFET technology is attractive. Although the controversial question about the intrinsic limit of ferroelectric dipole response was clarified [3, 4], the more systematic comparison on FinFET- and NC-FinFET-based ring oscillators (ROs) is required based on the state-of-the-art technology. There are some literatures discussing NC-FinFET circuit metrics [5–8]. However, the performance could be overestimated due to the uncalibrated capacitances and the presence of internal metal which theoretically eliminates hysteresis-free operation [9, 10]. Furthermore, the doping-related ferroelectric (FE) may also suffer from properties variations [11] and impact the variability in devices and circuits.

In this paper, we addressed the above questions by utilizing the TCAD simulations based on the advanced FinFET technology nodes and the calibrated compact models for circuit simulations, assuming that the FE can be properly integrated into those technologies. The results indicated the negligible impact of FE switching dynamics and FE property variations on devices and circuits.

II. DEVICE CALIBRATION AND SIMULATION METHODOLOGY
The in-house TCAD is first calibrated with 7-nm and 14-nm FinFET technologies ($V_{DD}$ = 0.75 and 0.8 V) for both $I_{DS-VGS}$ and $C_{GG-VGS}$, as shown in Fig. 1, with the FinFET geometry and electrical targets from the PDKs. The NC-FinFET performances of $P_r=10\ \mu\text{C}/\text{cm}^2$ and $E_C=1\ \text{MV/cm}$ (Fig. 2) are predicted by the TCAD which internally solving the Poisson and Landau-Khalatnikov equations self-consistently with only converting the high-κ dielectric to FE ($t_{high-\kappa}=t_{FE}$) by employing doping [12]:

$$V_{FE} = \text{Irr}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

where $\alpha$, $\beta$, and $\gamma$ are the ferroelectric material parameters which can be related to $P_r$ and $E_C$ [7]. For HfO$_2$-based FE ($\gamma=0$) assumed in this study, $\alpha = (-3\sqrt{3}/4) \cdot (E_C/P_r^3)$ and $\beta = (3\sqrt{3}/8) \cdot (E_C/P_r^3)$.

![Fig. 1: TCAD calibrations for (a) 7-nm and (b) 14-nm FinFETs (Symbols: PDK; lines: TCAD). (c) RLC sub-circuit model for FE dipole dynamic switching [3] coupled with DC NC-FinFET model. $E_{FE,avg}$ is the average of electric field at source and drain sides, and $\epsilon_{FE} = 16$ is the permittivity.](image-url)
The BSIM-CMG-based NC-FinFET compact model [13, 14], which spatially solves the electrostatics with Landau-Khalatnikov equations (a distributed model), was calibrated with the mentioned TCAD data (Fig. 2). The FE dynamic switching is modeled by an RLC sub-circuit with the viscosity parameter $\rho$ (the first order $dP/dt$ term) and the kinetic inductance parameter $l$ (the second order $d^2P/dt^2$ term) [3], as shown in Fig. 1 (c). The experimentally measured values of $\rho$ and $l$ by optical [3] and electrical measurement [15] are listed in Table I. The circuit performance is evaluated using a 7-stage FO4 ring oscillator with 10 fins for each transistor, and the impact of the load capacitance will be examined. The calibrated compact model is predictive for FE properties with only varying FE parameters by 10% (Fig. 2), which ensures the accuracy of variability modeling. The 7-nm and 14-nm FinFET PDKs enable the statistical global variations combined with the additional FE property variations in NC-FinFET, and thereby variability in ROs. Note that the threshold voltage ($V_{TH}$) of NC-FinFET is shifted to match the $I_{OFF}$ of reference FinFET for fair comparison of circuit performance metrics.

### III. RESULTS AND DISCUSSION

#### A. Ring Oscillator Analysis

Fig. 3 shows the impact of the FE dynamic switching parameters $\rho$ and $l$ on delay and EDP of (a) 7-nm and (b) 14-nm ring oscillators [C$_{load}$ = 1f (F)], showing $l$ term is negligible. Only small penalty on delay and EDP is observed with reported $\rho$ and $l$ values [3].

The BSIM-CMG-based NC-FinFET compact model [13, 14], which spatially solves the electrostatics with Landau-Khalatnikov equations (a distributed model), was calibrated with the mentioned TCAD data (Fig. 2). The FE dynamic switching is modeled by an RLC sub-circuit with the viscosity parameter $\rho$ (the first order $dP/dt$ term) and the kinetic inductance parameter $l$ (the second order $d^2P/dt^2$ term) [3], as shown in Fig. 1 (c). The experimentally measured values of $\rho$ and $l$ by optical [3] and electrical measurement [15] are listed in Table I. The circuit performance is evaluated using a 7-stage FO4 ring oscillator with 10 fins for each transistor, and the impact of the load capacitance will be examined. The calibrated compact model is predictive for FE properties with only varying FE parameters by 10% (Fig. 2), which ensures the accuracy of variability modeling. The 7-nm and 14-nm FinFET PDKs enable the statistical global variations combined with the additional FE property variations in NC-FinFET, and thereby variability in ROs. Note that the threshold voltage ($V_{TH}$) of NC-FinFET is shifted to match the $I_{OFF}$ of reference FinFET for fair comparison of circuit performance metrics.

### TABLE I

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$\rho$ (Ω·m)</td>
<td>0.0018</td>
<td>0.0022</td>
</tr>
<tr>
<td>$l$ (H·m)</td>
<td>50 $\times$ 10$^{-18}$</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Fig. 3: Impact of $\rho$ and $l$ on normalized delay and EDP of (a) 7-nm and (b) 14-nm ring oscillators [C$_{load}$ = 1f (F)], showing $l$ term is negligible. Only small penalty on delay and EDP is observed with reported $\rho$ and $l$ values [3].
values of $\rho = 0.0018$ (Ω·m) and $l = 50 \times 10^{-18}$ (H·m) as denoted by white dots in Fig. 3.

Fig. 4 (a) and (b) show the delay versus leakage power and EDP versus $V_{DD}$ curves of 7-stage FO4 ROs consisting of the 7-nm/14-nm FinFETs with 3σ FE variations of 0% and 10% (1000 samples). Note that the FE thickness variation is assumed the same as HfO$_2$ variation in FinFET technology.

is observed in the 7-nm case where the $V_{DD}$ of NC-FinFET can be scaled from 0.75 V down to 0.63 V. Although there is a penalty on $C_{eff} = EDP/(V_{DD}^2)$ of NC-FinFET, the compensation of better $K_{eff}$ (=$\tau/C_{eff}$) leads to scaled $V_{DD}$ and thus energy-efficiency. At high load of $C_{load} = 4f$ (F), the energy saving of 7-nm/14-nm NC-FinFET is even more significant (32.7%/23.7%) with the further scaled $V_{DD}$ of 0.59 V/0.66 V because of higher drive current of NC-FinFETs [see Fig. 5 (a) and (b)] to charge/discharge the parasitic capacitance. The results are summarized in Table II. However, $C_{load} = 0.1f$ (F) (low load) leads to energy inefficiency due to NC-enhanced gate capacitance of NC-FinFET (Fig. 2). For 7-nm/14-nm NC-FinFET with low load, scaling $V_{DD}$ from 0.75 V/0.8 V to 0.65 V/0.7 V under iso-delay leads to the similar energy and 6% more energy consumptions, respectively.

B. NC-FinFET Variability

The variance in ferroelectric properties $P_t$ and $E_C$ are inevitable due to doping and strain variations [11]. Fig. 6 shows statistics of $I_{ON}$, $I_{OFF}$, $C_{OV}$, $C_{GG}$, SS, and DIBL with $P_t$ and $E_C$ variation of 3σ = 0%, 5%, and 10% combined with the FinFET statistical global process variations for 7-nm/14-nm technologies. The FE thickness variation is considered the same as high-κ dielectric variation due to the similar atomic layer deposition (ALD) process [16, 17] with other process modules being fixed. The $I_{OFF}$ of NC-FinFETs are relatively sensitive to the FE variation due to the inner fringing-induced change in $V_{TH}$ [14] and thus exponential impact on $I_{OFF}$. Since the SS and DIBL for the nominal NC-FinFET are low enough to 60 mV/dec and < 5 mV respectively, the FE variation does not impact the SS and DIBL much. As long as the 3σ variation of FE is less than 25% suggested in [11], the FE variations in other device metrics of both technologies are insignificant, showing the greater impact of FinFET inherent variations from PDK. Thus, it is expected that FE variations in general do not influence the RO delay and energy with a reasonably controlled ALD process and integration for FE as summarized in Table III.

IV. CONCLUSION

Although the process integration of NC-FinFET into the state-of-the-art technology requires more engineering effort, the preliminary circuit performance evaluation is demanded.
The analysis of NC-FinFET-based ring oscillators shows that the ferroelectric dynamic switching effect is negligible with the experimentally measured parameters and the NC-FinFET enables energy saving by reducing $V_{DD}$ without any delay penalty for advanced technology nodes due to its superior drive current. Furthermore, coupled with the FinFET variation from PDK, the FE variability may not have a great impact on the ring oscillator performance. However, further experimental study on FE process integration and its impact on NC-FinFET is an important topic for future work.

REFERENCES


