Multi-Domain Ferroelectric FETs with Negative and Enhanced Positive Capacitance for Logic Applications

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***Abstract*—In this paper, we analyze the multi-domain (MD) ferroelectric FET (FEFET) as a non-hysteretic transistor with enhanced gate control for standard logic applications. We consider two regimes of operation i.e., when the ferroelectric (FE) layer acts as (1) an effective negative capacitor (NC) under soft domain-wall (DW) displacement and (2) an enhanced positive capacitor (EPC) in case of hard-DW with no displacement. Our analysis is based on the self-consistent 2D phase-field simulation of FEFET considering HZO as the FE layer. We analyze the MD induced non-homogeneous potential profile in FEFET and show that the MD NC and EPC phenomena lead to an improvement in the subthreshold-swing and mitigation of other short-channel effects compared to the conventional high-k FET (HKFET). Moreover, the presence of domain-wall (DW) and non-homogeneous potential profile in the FEFET channel leads to a unique transport and a robust gate length scaling behavior compared to the HKFETs, which signifies the benefits of MD FEFET for future scaled FET technologies.**

Keywords—Ferroelectric, FeFET, Fe-Fin-FET, Scaling, Voltage Amplification, Multi-domain, Domain-Wall, Negative-Capacitance, Permittivity Enhancement.

I. Introduction

Ferroelectric based field-effect-transistors (FEFET) employing $Hf_{1-x}Zr_xO_2$ (HZO) as the FE layer are emerging as one of the most promising candidates for future electronics [1-4]. Besides non-volatile memory attributes, FEFET has been demonstrated to offer non-hysteretic logic behavior [2] signifying enhanced gate control and better performance compared to the conventional high-k FET (HKFET) with HfO_2 gate insulator. Under certain conditions, the FE layer in FEFET can potentially exhibit a non-hysteretic negative capacitance (NC) effect and such an FEFET is usually referred to as NCFET [3]. While the NC effect was initially proposed and has been extensively investigated in the context of a single-domain ferroelectric [3], another possible mechanism for a quasi-static and hysteresis-free NC effect (especially for HZO with low gradient energy coefficients) is polarization switching in multi-domain FE via soft domain-wall (DW) displacement [6-7]. While in the NC regime for soft DW, the effective permittivity of the FE layer becomes negative, it has been shown that the effective permittivity of the FE layer can also *enhance but remain positive* due to the electrostatic interactions among multi-domain states. Such enhanced positive capacitance

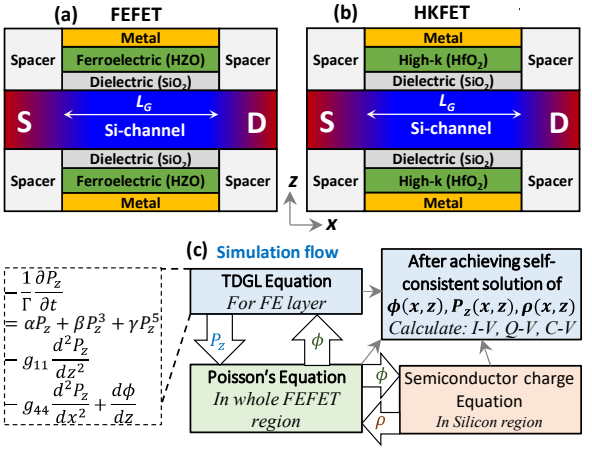

Figure 1: (a) FEFET (with HZO as gate insulator) and (b) HKFET (with HfO_2 as gate insulator) device structure. (c) Simulation flow used in phase-field simulation of FEFET/HKFET. Note: The TDGL module is excluded for HKFET simulation.

(EPC) effects in FE appear in densely patterned MD states with hard domain-wall and in the absence of polarization switching [4,7]. While both the multi-domain NC effects and EPC effects have been speculated to yield superior performance in FEFETs, the implications of multi-domain states in the FE layer from the perspective of FEFET operation have not yet been fully investigated. To that end, in this paper, we investigate the implication of the multi-domain NC effect and EPC effect on FEFET characteristics by employing extensive phase-field-based device simulation. In addition, we analyze the short channel effects in multi-domain FEFET for logic applications (Fig. 1(a)) and compare its performance with the conventional HKFET (Fig. 1(b)) with HfO_2 as the gate insulator.

II. Phase-field Simulation Framework of FEFET

In our phase-field simulation, we self-consistently solve the 2D time-dependent Ginzburg-Landau (TDGL) equation for polarization (P), Poisson's equation for potential (ϕ) and charge/transport equations for charge density profile in the semiconductor (Si) region [4]. The TDGL equation incorporates the free energy, gradient energy along the FE thickness and length, and depolarization energy in the FE layer. The long-range Coulomb interaction among polarization-induced bound charges is captured via Poisson's equation. The simulation flow is shown in Fig. 1(c).

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We consider the *P* direction in FE to be along the film thickness, which is analogous to the c-axis of its orthorhombic crystal phase. The simulation parameters and the calibration with experiments can be found in our previous paper [4]. Note that the Landau coefficients used in our simulation are assumed to be strain normalized based on the assumption of a stress-free interface. Also, note that the HZO film is well-known to exhibit polycrystallinity [8] and the HZO-SiO_2 interface yields charge trapping/de-trapping [9]. However, for simplicity, here, we do not consider such polycrystallinity and charge trapping effects in the HZO-SiO_2 interface.

It is well known that the FE layer in the gate-stack of FEFET exhibits depolarization-field due to the presence of underlying dielectric (DE: SiO_2) and Si layer. In our earlier work [4], we discuss that, to suppress the depolarization energy, the FE layer breaks into multi-domain (MD) state with alternating *P* directions. Such an MD state allows the formation of in-plane electric-field (between neighboring domains) and thus suppresses the depolarizing electric-field within the FE layer. Further, the nature of domain-wall (DW), as well as the domain density, depends on the FE thickness (T_{FE}) [4,7]. For HZO, in case of T_{FE} <1.5nm, the type of DWs is soft and the *P*-switching via soft-DW displacement is non-hysteretic due to zero (or infinitesimally small) coercive field of soft-DW motion. Such soft-DW displacements lead to the hysteresis-free NC effect in the FE layer and the effective permittivity of the FE layer becomes negative. Therefore, in this work, we consider the HZO thickness of 1.2nm for analyzing the FEFET with MD NC effects. In contrast to the soft-DW, for HZO thickness above 1.5nm, the nature of DW becomes hard. *P*-switching via hard-DW displacement is hysteretic due to the non-zero coercive field of hard-DW motion. While the *P*-switching via hard-DW displacements leads to the hysteretic NC effect, it has been shown that for a limited voltage window, when there is no *P*-switching, a non-hysteretic operation can be obtained. More importantly, in this regime, the effective permittivity of the FE layer enhances but remains positive (EPC effect). The enhancement in effective permittivity is due to the fact that some in-plane electric field lines near the domain walls are transformed to out-of-plane fields on the application of gate voltage, which induces an additional charge in the gate stack (more details in [4,7]). Moreover, such a non-hysteretic EPC effect increases with the T_{FE} scaling as the domain density increases with the decrease in T_{FE}. Therefore, in this work, we consider the HZO thickness of 2.4nm for analyzing the FEFET characteristics with the EPC effect. For comparing these FEFET characteristics with conventional HKFETs, we replace the HZO layer with HfO_2 having the same physical thickness.

III. Multi-Domain FEFET with NC Effects

For the simulation parameters considered, the FE layer in FEFET exhibits soft-DW for T_{FE}=1.2nm that undergoes

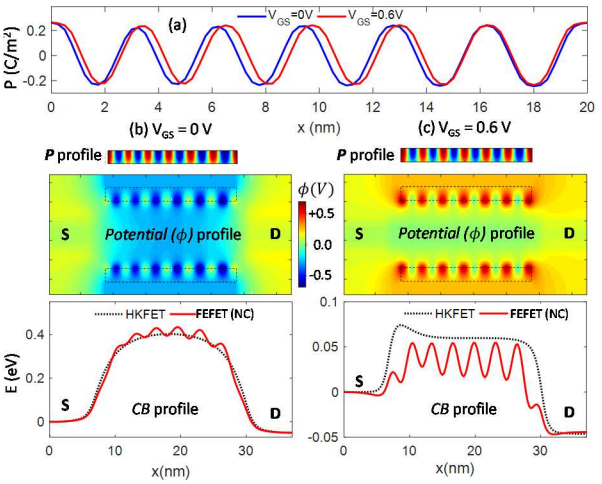

Figure 2: Polarization (*P*) profile of FE layer (near the FE-DE interface) of FEFET (with 1.4nm HZO) showing gate voltage (V_{GS}) driven soft-DW displacement based *P*-switching. *P* map in FE, potential (ϕ) profile of FEFET and conduction band (CB) profile of FEFET and HKFET at (b) V_{GS} = 0V and (c) V_{GS} = 0.6V. Here, V_{DS} = 0.05V.

soft-DW displacement under the influence of applied V_{GS} (Fig. 2(a)). Our results in Fig. 2(a) show that the DW displacement is less dominant on the drain side of the FE layer (right) compared to the source side (left) as $V_{GD}<V_{GS}$ ($V_{DS}>0$). Interestingly, the presence of the MD state in the FE layer leads to a significantly non-homogeneous potential profile in the underlying Si channel due to the spatially varying *P*-induced bound charges at the HZO-SiO_2 interface. Therefore, the HZO-SiO_2 interface potential (V_{INT}) and the SiO_2-Si surface potential (ψ_s) also becomes non-homogeneous. Similarly, the conduction-band (CB) profile of FEFET in Si (0.5nm away from Si-SiO_2 interface) shows ripples (Fig. 2(b-c)). Here, the peaks (valley) in the CB profile of Si signify the presence of the -P (+P) domains in the FE layer above. In the OFF state (V_{GS}=0V), the CB maxima in FEFET is higher compared to the HKFET and thus the OFF-state current of FEFET is lower compared to the HKFET (Fig. 3(a)). Similarly, in the ON state (V_{GS}=0.6V), the CB maxima in

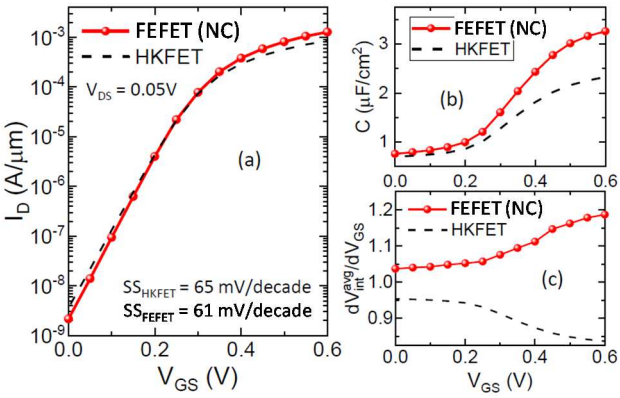

Figure 3: (a) I_D-V_{GS} and (b) *C*-V_{GS} characteristics of FEFET and HKFET signifying improved gate control and reduced SS in FEFET. (c) Differential change in average HZO-SiO_2 (HfO_2-SiO_2) interface potential in FEFET (HKFET) with respect to V_{GS}.

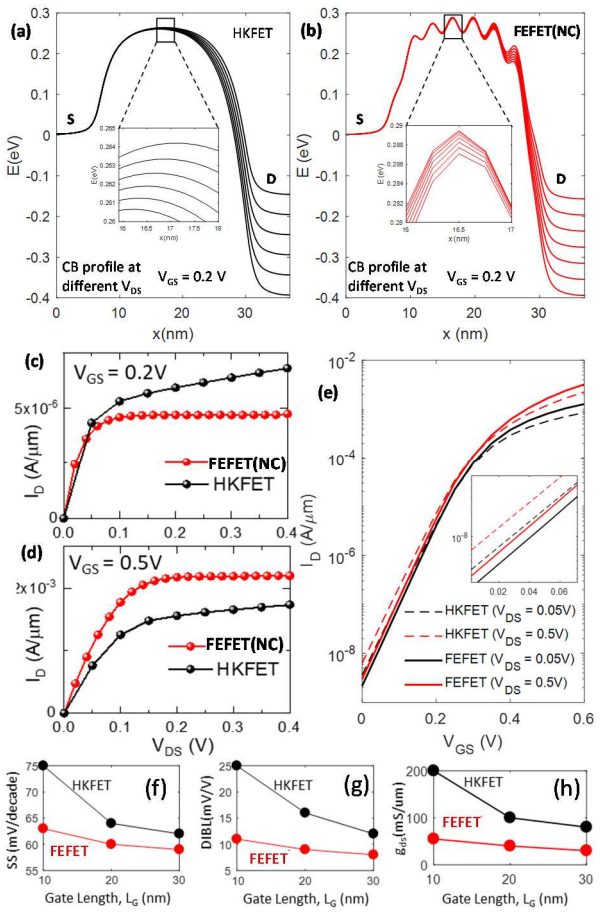

Figure 4: CB profile of (a) HKFET and (b) FEFET with NC effect at different V_{DS} and V_{GS} = 0.2V. I_D-V_{DS} characteristics of FEFET and HKFET at (c) V_{GS} = 0.2V and (d) V_{GS} = 0.5V signifying a decreased output conductance (g_{ds}) in FEFET compared to HKFET. (e) I_D-V_{DS} characteristics at different V_{DS} signifying reduced DIBL in FEFET compared to HKFET. (f) Subthreshold-swing (SS), (g) DIBL and (h) g_{ds} of FEFET and HKFET for different gate length (L_G).

FEFET is lower compared to the HKFET and hence, the ON state current of FEFET is higher (Fig. 3(a)). Further, the subthreshold-swing (SS) of FEFET is 61mV/decade which is lower than the 65mV/decade SS of HKFET. Such SS reduction and I_{ON}/I_{OFF} enhancement in FEFET can be understood from the capacitance (C) versus V_{GS} characteristics of FEFET in Fig. 3 (b) that signifies higher gate capacitance in FEFET (1.5x) compared to the conventional HKFET. Such capacitance enhancement originates due to the MD NC effect of the FE layer. To validate that, we plot the differential change in HZO-SiO_2 interface potential averaged along the length (V_{INT}^{avg}) with respect to V_{GS} in Fig. 3(c). We can see that, for FEFET dV_{INT}^{avg}/dV_{GS}>1, where for HKFET dV_{INT}^{avg}/dV_{GS} <1. This implies that the effective capacitance of the HZO layer is negative in FEFET.

Now, let us analyze the influence of drain voltage (V_{DS}) in FEFET with NC effect. The CB profiles of FEFET and HKFET at different V_{DS} are shown in Fig. 4(a) and Fig. 4(b), respectively. Note that the CB profile of HKFET exhibits only one maximum which decreases with the increase in V_{DS}. This leads to a finite output conductance (g_{ds}) in the I_D-V_{DS} characteristics of HKFET. However, in FEFET, due to the presence of the MD state in FE, the CB profile exhibits several local maxima along the gate length direction. In such a scenario, an increase in V_{DS} mostly reduces the CB peaks near the drain side but causes a negligible change near the source side. This is because the V_{DS}-induced electric field can be compensated by the (i) local change in P magnitude in the FE layer near the drain side and (ii) higher local charge in the Si in the valley of rippled CB profile near the drain side. Therefore, the penetration of the drain-induced field towards the source side is somewhat shielded. As the CB peaks in the FEFET near the source side do not significantly depend on V_{DS} in the saturation region, therefore, FEFET exhibits significantly lower g_{ds} ($=dI_D/dV_{DS}$) compared to the HKFET (Fig. 4(c-d)). Due to a similar rationale, the drain-induced barrier lowering (DIBL) in FEFET is reduced compared to the HKFET as shown in Fig. 4(e). Such a unique feature of the MD FE further leads to important trends in the context of gate length scaling. The SS, DIBL and g_{ds} of FEFET and HKFET for different gate lengths (L_G) are shown in Fig. 4(f) signifying that the short-channel effect in FEFETs does not significantly increase with the gate-length scaling compared to HKFET (similar to the experimental results in [10]). This is due to the shielding nature of the MD FE for the drain induced field within the channel of FEFET as discussed above.

IV. Multi-Domain FEFET with Enhanced Positive Capacitance Effects

To investigate the FEFET characteristics featuring EPC effect, we consider the HZO thickness of 2.4nm while keeping all the other device parameters the same as before. The simulated polarization profile of the FEFET gate stack (Fig. 5(a)) suggests the formation of MD state with hard-DW and the absence of P-switching in the FE layer for the applied V_{GS} range (less than the coercive voltage of the FEFET). Therefore, in response to V_{GS}, we only observe the magnitude change in local P but no directional change (Fig. 5(a)). The simulated I_D-V_{GS} and C-V_{GS} characteristics of FEFET and HKFET are shown in Fig. 5(b-c) signifying that the FEFET exhibits better gate control (lower SS, higher I_{ON}/I_{OFF}) and higher C compared to HKFET (with HfO_2 thickness=2.4nm). Note that, the differential change in FE-DE interface potential (dV_{int}^{avg}/dV_{GS}) in this hard-DW (without P- switching) case is <1 but higher than the HKFET (Fig. 5(d)). Therefore, this performance enhancement in FEFET is due to the EPC effect, and *not* due to the NC effect. It is also important to note that lower short channel effects and higher C due to EPC are not merely due to higher intrinsic permittivity of HZO compared to HfO_2, but also due to the transformation of in-plane electric fields to the out-of-plane fields near the DWs, as discussed before.

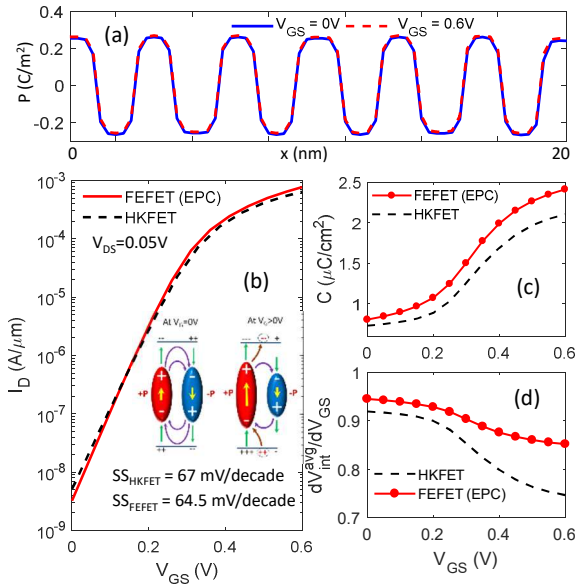

Figure 5: FEFET with EPC (hard-DW: T_{FE} = 2.4nm). (a) *P* profile of FE layer showing V_{GS} driven small change in *P* magnitude (no DW displacement) (b) I_D-V_{GS} and (c) *C*-V_{GS} characteristics of FEFET (2.4nm HZO) and HKFET (2.4nm HfO_2). (d) Differential change in average HZO-SiO_2 (HfO_2-SiO_2) interface potential in FEFET (HKFET) with respect to V_{GS}.

Now, let us analyze the influence of V_{DS}. Similar to the FEFET with NC effects (T_{FE}=1.2nm), the FEFET with EPC effect exhibits lower output conductance (g_{ds}) in the I_D-V_{DS} characteristics compared to HKFET (Fig. 6(b)). This is because of the (i) higher capacitance of HZO-SiO_2 stack (Fig. 5(d)) in FEFET compared to HfO_2-SiO_2 stack in HKFET, (ii) higher local charge in the Si channel (in the valley of rippled CB profile near the drain side) (Fig. 6(b)). Therefore, similar to the FEFET with NC effect, the penetration of drain induced field towards the source side is somewhat shielded in FEFET with EPC effects. Similarly, FEFET with EPC also shows reduced DIBL compared to HKFET. Furthermore, EPC-FEFETs (like NC-FEFETs) exhibit improved gate length scalability compared to HKFETs.

While both the FEFET with NC and EPC effects exhibits reduced SS, DIBL, and g_{ds} compared to the HKFET with the same physical oxide thickness, some key differences must be emphasized. First, the NC effect requires *P*-switching (directional change in local *P*) in the FE layer, while the EPC effect occurs in absence of *P*-switching. Second, the effective permittivity of the FE layer is negative for the NC effect while it is positive (but enhanced) for the EPC effect. Third, the effective capacitance of the HZO-SiO_2 is higher than the SiO_2 capacitance for NC but lower for EPC. Therefore, for NC effect $dV_{INT}^{avg}/dV_{GS} > 1$ while for EPC effect $dV_{INT}^{avg}/dV_{GS} > 1$. Due to these differences, the reductions in SS, DIBL, and g_{ds} for NC-FEFET are more prominent compared to the EPC-FEFET.

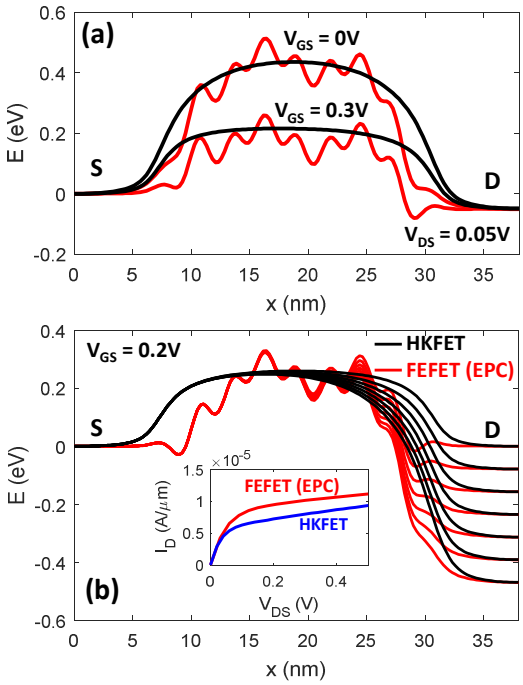

Figure 6: CB profile of FEFET (2.4nm HZO) with EPC effect and HKFET for different (a) V_{GS} and (b) V_{DS}. The I_D-V_{DS} characteristics of FEFET and HKFET are shown at the inset of (b) signifying lower g_{ds} in FEFET.

V. Conclusion

We analyzed the multi-domain FEFETs with soft-DW induced negative capacitance and hard-DW induced enhanced positive capacitance effects. Our analysis suggests that both the MD NC and EPC effect leads to improved FEFET characteristics compared to conventional HKFETs. We show that the multi-domain FE-induced rippled potential profile in the channel plays a vital role in improving the short-channel effects in FEFETs and leads to superior gate length scalability.

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