Miller-Capacitance Analysis of High-Voltage MOSFETs and Optimization Strategies for Low-Power Dissipation

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***Abstract*—High voltage MOSFETs are widely used for bias ranges of a few dozens of volts to a few hundred of volts. The trench-type MOSFET is one of the key devices for realizing this wide range applications. However, the device characteristics are not yet well understood, especially, the Miller-capacitance variation for different device structures is still mysterious. Here we show, that the capacitance variation is very much dependent on the applied device structure. An observed capacitance increase as a function of V_{ds}, contrary to the conventional decreasing trend, is due to the large induced field within the highly resistive drift region. A narrow width of the drift region in a super-junction structure will easily become fully depleted, due to the junction between drift and pillar region of the substrate, which causes a fully depleted condition. This full-depletion situation induces a high field within the drift region, resulting in a potential increase even at the gate oxide.**

Keywords—High voltage MOSFETs, Miller capacitance, analytical model, super junction

I. Introduction

High voltage MOSFETs are key devices in power-electric systems, helping to mitigate global-warming problems. Many structural variations are possible for a wide range of application-bias conditions [1]. Our focus is given on the Miller capacitance, which plays a major role for the power consumption [2]. It has been found, that the Miller capacitance C_{gd} can be in general expected to reduce gradually, when V_{ds} increases. However, it has been also observed, that C_{gd} can increase under certain conditions. Such an increase causes a higher total power consumption, and thus complicates power-circuit design by requiring a compromise among device performances. For this reason, an accurate compact C_{gd} model is necessary. Unfortunately, the origin of the observed variations in the C_{gd} characteristics is not yet clear. Here we have found a strong dependence of the C_{gd} characteristics on the MOSFET structure, originating from the structural-boundary-condition influence on the depletion-width extension within the drift region, when sustaining high applied voltages. These structural boundary conditions influence the 2D potential distribution, which is modeled as a potential redistribution within the model framework. A major effect of the potential redistribution due to the structural limitations can be a restriction of the potential increase, which then results in an abnormal increase of the depletion width, externally observed as a C_{gd} increase. The developed compact model for this effect has been implemented in HiSIM_HV [3] for accurate prediction of the power dissipation of circuits, and can further be applied to a device-structure optimization for realizing circuitry with lower power consumption.

II. Analysis and Modeling of CGD

A. Structural Feature of SJ-MOSFET

The investigation was performed with 2D-device simulation [4]. Fig. 1 shows the C_{gd} characteristics as a function of V_{ds} for different structural variations (see Fig. 1b). As the basic structure, a Super-Junction MOSFET structure [5]-[7] is used, which provides a general HV-MOSFET structure being applicable in applications up to extremely high voltages. The trench width W_{trench} and the pillar width W_{pillar} have been varied so that the origin of the C_{gd} variation can be addressed. It can be seen that the structural variation is the origin of the C_{gd} variation. Fig. 2 shows the 2D distribution of the depletion boundary for different V_{ds} at V_{gs} = 0 V, (a) for ST00 and (b) for ST11. Each line refers the depletion boundary for each V_{ds} value. The outer lines in both, drift and pillar regions, refer to the boundaries at V_{ds} = 100 V, and the lines toward the junction are the boundaries at reduced V_{ds} down to 2 V. Fig. 2a illustrates the saturated depletion extension for increased V_{ds} from the same depletion boundary for different V_{ds} values due to the relatively narrow width W_{drift} of 1 μm, which limits the depletion-width extension along the vertical direction W_{dw}. On the contrary, Fig. 2b shows

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the extension of the depletion boundary with increased V_{ds} for wide width W_{drift} of 4 µm.

B. Origin of C_{gd} Increase

Fig. 3 shows potential-distribution comparisons between ST00 and ST11. Though the potentials along the A-B line and the C-D line (see Fig. 2b) are independently distributed for ST11, both distributions are verified to extend deeply into the device middle for ST00. Fig. 4 compares the potential distributions in vertical direction along the E-F line at position of 5 um at the middle of the device length. It can be seen that the potential difference from E to F is less than 30 V for ST00. This difference remains the same also for higher V_{ds} values. On the contrary, this difference varies substantially as a function of the V_{ds} values for ST11. The reason for the observed behavior is that the structure-induced limitations of the depletion extension lead to a constant potential drop at the *p/n* junction along the vertical direction, which results in the synchronized potential distributions along the A-B line and the C-D line (see Fig. 3a).

C. Depletion-Width Extension as a Function of V_{ds}

Fig. 5 depicts the depletion width as a function of V_{ds} for the four different structures shown in Fig. 1b. In case of ST11, the depletion extension shows conventional characteristics. However, it increases drastically as the depletion extension is restricted by the structural limitation at $V_{ds} > 25$ V, which coincides with the V_{ds} value when the potential distribution departs from the conventional one. The observed depletion extension is confined by the potential distribution to keep the vertical depletion width extension within W_{drift}, and is caused by a potential redistribution necessary to synchronize the distributions along the A-B line and the C-D line, in order to keep the depletion-width extension W_{dw}, vertical to the drift/pillar junction, within W_{drift}. As a consequence, the depletion extension along the A-B direction, due to the 2D effect of the potential distribution, is the origin of the C_{gd} increase for the narrow structure of ST00. Thus, describing the potential distribution shown in Fig. 3 analytically is the modeling task.

The potential redistribution along the A-B line as well as the C-D line for the narrow W_{drift} and W_{pillar} cases (ST00, ST01, ST10) can be modeled by simplifying, that the drift region as well as the pillar region are mostly depleted under high V_{ds}. Thus, a linear potential distribution can be approximated, which results in a constant electric field, described by the drift length and the potential difference between the internal potential value at the channel/drift junction and V_{ds}, as schematically shown in Fig. 6. The linear potential distribution, together with the potential value induced by the gate voltage, determines the final potential distribution as observed in Fig. 5. The depletion width, calculated with use of the potential distribution, is compared to the 2D-device simulation result in Fig. 7.

D. Modeling of C_{gd} Increase

It is normally expected, that C_{gd} reduces monotonically to zero, when the depletion extension reaches the drain contact. Commonly, the device length is rather long and C_{gd} is kept at a finite value even for large V_{ds}, as seen in Fig. 1a for ST10 and ST11. Since the depletion extension along the vertical direction enters the fully depleted condition for the ST00 and ST01 cases, an abrupt reduction of C_{gd} to zero should result. However, C_{gd} starts to increase due to the depletion extension along the device length, which is caused by the synchronization of the potential distributions along the A-B line and the C-D line, for keeping the potential difference at the V_{ds} value, providing the fully-depleted condition. Furthermore, this synchronization becomes tight, if both W_{drift} and W_{pillar} are narrow. By increasing the W_{pillar} width, namely for the ST01 case, the potential distribution along the C-D line is nearly unchanged in comparison to that of the ST11 case and the synchronization with the A-B line happens only near to the drain contact, as can be expected and shown in Fig. 5. However, the C_{gd} characteristics are similar to that of the ST00 case. The reason is, that the C_{gd} increase occurs due to an additionally induced charge, as depicted in Fig. 8. Origin of the additional charge is the high field, induced within the drift region, as seen in Fig. 3, along the A-B line. The surface-potential value in the drift region is governed mostly by the gate voltage together with V_{ds}, which transits smoothly to a linear distribution within the drift region. During the transition, the surface-potential value itself at the surface is influenced by the high field, causing the additionally induced charge. The V_{ds} value is the value calculated with use of the continuity relationship along the device, namely V_{DP} in Fig. 6. It can be concluded, that the C_{gd} increase is due to the fully-depleted condition, caused within the drift region, and thus the phenomenon can be observed only for ST00 and ST01 of our studied cases.

III. Discussion and Conclusion

The Millar capacitance C_{gd} is a key value, determining the power loss of circuits. Unfortunately, C_{gd} is not always decreasing as a function of the drain voltage, as conventionally observed, but even an increase is often observed. Here we found, that the reason for such an C_{gd} increase is the field increase due to the fully-depleted condition within the drift region, induced by a relatively narrow trench width in combination with relatively high V_{ds}. Modeling has been done by assuming a linear potential increase within the drift region, which causes an additional potential increase at the trench surface in addition to the potential determined by the gate voltage.

To avoid the C_{gd} increase for realizing low power circuit operation, a device structure optimization must be done under consideration of the bias conditions. Especially, the width of the drift region and its impurity concentration must be carefully optimized. Our developed model requires only one model parameter to adjust an additional simple linear potential distribution along the device, which can reproduce the observed C_{gd} variations for different structural variations. Therefore, it can be concluded that the developed model is applicable for the device optimization.

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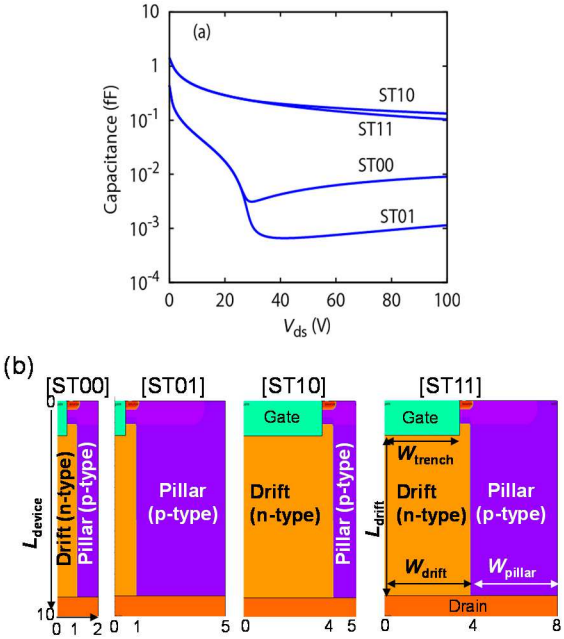

Fig. 1. (a) The Miller capacitance C_{gd} as a function of V_{ds} at V_{gs}=0 for different device structures with different W_{drift} and W_{pillar}, (b) four structural variations, where the drift width W_{drift} and the pillar width W_{pillar} are set to either of narrow (1µm) or wide (4µm) case.

TABLE I. LIST OF DEVICE PARAMETERS

Device parameter	Device structure			
	ST00	ST01	ST10	ST11
L_{drift} (um)	7.4	7.4	7.4	7.4
W_{trench} (um)	0.5	0.5	3.5	3.5
W_{drift} (um)	1	1	4	4
W_{pillar} (um)	1	4	1	4

N_{drift} (cm^{-3}) Dopant concentration in the drift region $2 \cdot 10^{16}$
N_{pillar} (cm^{-3}) Dopant concentration in the pillar $2 \cdot 10^{16}$

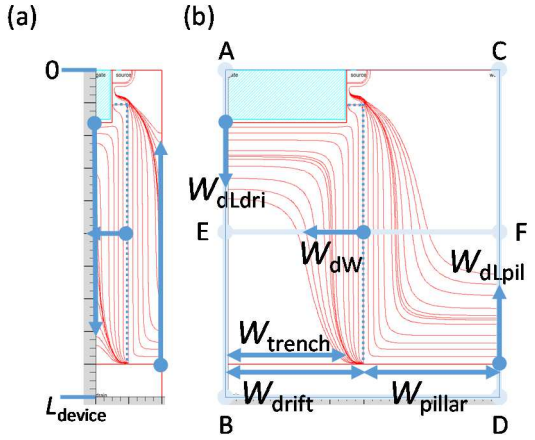

Fig. 2. 2D boundary distributions of the depletion extension for different V_{ds} at V_{gs}=0, (a) for ST00 and (b) for ST11. The overlap width (W_{drift} - W_{trench}) is kept the same for the two cases. W_{dw} is, in the text, termed "vertical" extension of depletion layer.

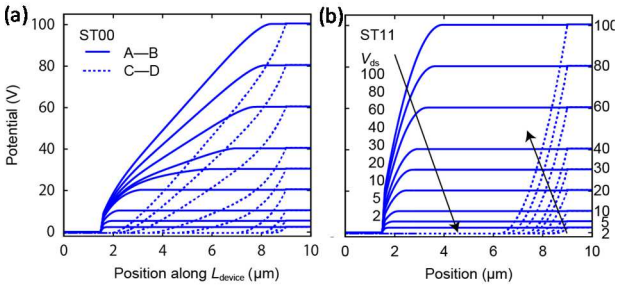

Fig. 3. Comparison of the potential distribution along the A-B line and the C-D line (see Fig. 2b), (a) for ST00 and (b) for ST11.

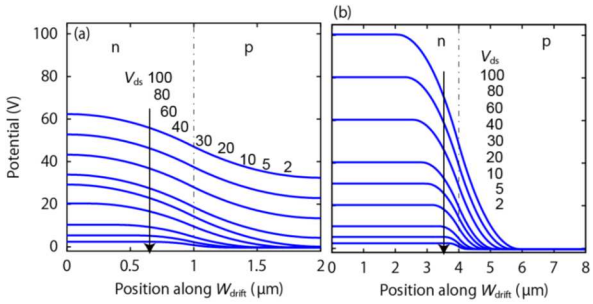

Fig. 4. Potential distribution along the transverse E-F line (see Fig. 2b) at the position of 5um, (a) for ST00 and (b) for ST11. The dash-dot line indicates the p/n junction between drift (n-type) and pillar (p-type) regions. Both drift and pillar are narrow for ST00, while both are wide for ST11. In (a), for ST00, the voltage drop across the p/n junction reaches the drain-bulk voltage at lower V_{ds} up to about 25 V. Above that, for V_{ds}= 30, 40, 60, 80, and 100 V (top 5 curves in (a)), the voltage drop across the junction retains a certain constant swing (about 30 V). The potentials on both sides (drift and pillar) continue to increase in a synchronized manner. In (b), for ST11, the voltage drop across the junction reaches V_{ds}. The potential on the pillar side stays at the lowest level (due to grounded body terminal), while the potential on the drift side matches the increased V_{ds}, without any of the constraint symptoms observed in (a).

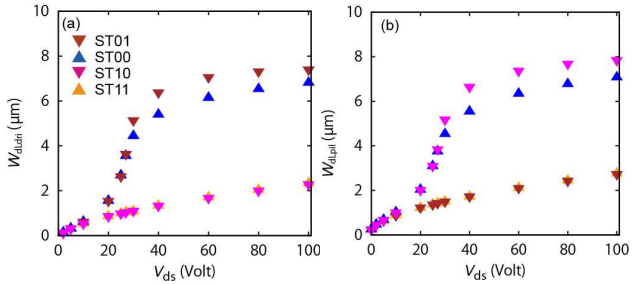

Fig. 5. Depletion-width extension as a function of V_{ds} for the studied structures, (a) along the A-B line and (b) along the C-D line. A monotonical increase is exhibited with respect to V_{ds}, when the drift region is wide (ST10 and ST11 for WdLdri) or when the pillar is wide (ST01 and ST11 for WdLpil), while it exhibits an offshoot increase at a threshold bias point and holds on at a larger level when the drift region is narrow (ST00 and ST01 for WdLdri) or when the pillar is narrow (ST00 and ST10 for WdLpil).

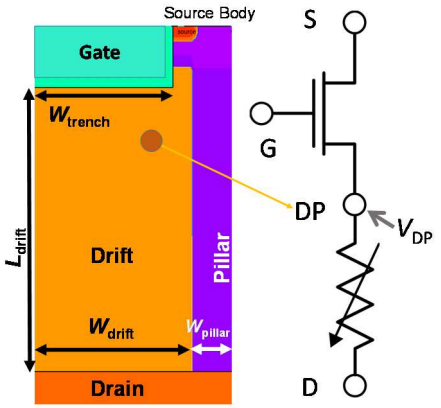

Fig. 6. Device structure and compact model represented by an equivalent circuit.

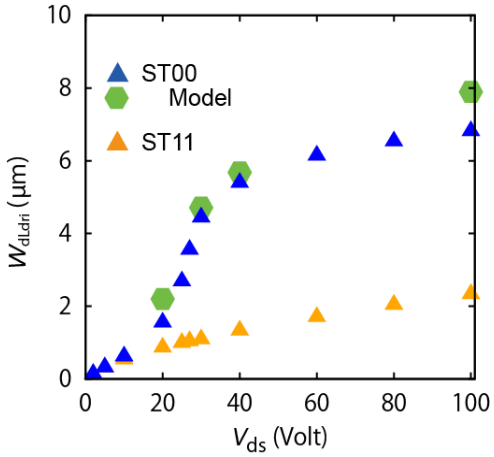

Fig. 7. Depletion-width extension as a function of V_{ds} for ST00 and ST11. Recapped partial plot of Fig. 5, accompanied by an estimated depletion width extension for ST00. The developed model captures the onset of the depletion-width increase, offshoot from ST11 at about V_{ds}=20 V, and the subsequent plateau.

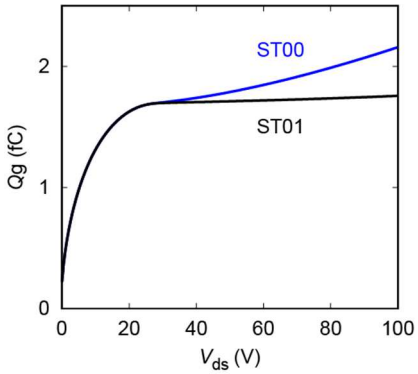

Fig. 8. Gate charge as a function of V_{ds} for the studied structures, ST00 and ST01. At a certain bias point along V_{ds}, the gate charge for ST00 (blue line) starts to deviate upward from that for ST01.

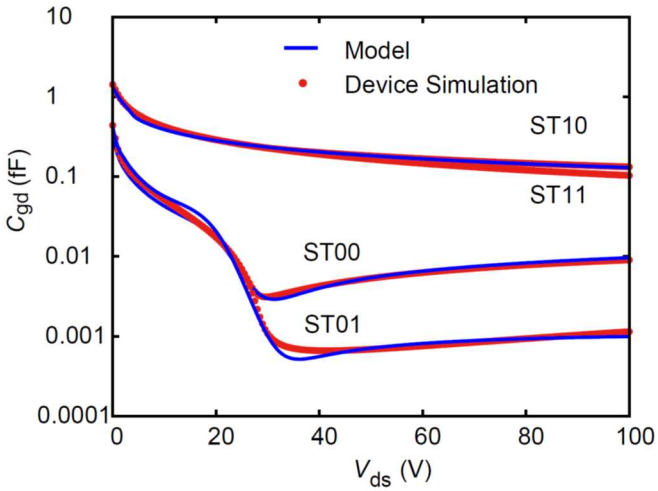

Fig. 9. Gate-drain capacitance fitted to device simulation results for the studied structures.