3D Electro-optical Simulations for Improving the Photon Detection Probability of SPAD Implemented in FD-SOI CMOS Technology

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***Abstract*—In this article, a 3D electro-optical simulation method is presented in order to estimate the Photon Detection Probability (PDP) of Single-Photon Avalanche Diodes (SPAD). The efficiency of the proposed simulation flow is demonstrated through a complete study aimed at improving the PDP of a SPAD implemented in 28nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology using a light-trapping approach (thanks to the patterning of Shallow Trench Insolation – STI layer). Simulation shows an increase of PDP spectrum of over 50% at wavelengths of 400-550nm and 750-1000nm and of 10-15% at the wavelengths of 550-750nm, compared to a reference SPAD without any nanostructuration.**

***Keywords*—SPAD; 28nm FD-SOI CMOS; Photon Detection Probability PDP; TCAD simulation; light-trapping**

I. INTRODUCTION

Single-Photon Avalanche Diodes (SPAD) or Geiger-mode Avalanche Diodes have been a very active research topic for the last few years due to their relatively simple structure making them easy to be implemented in CMOS technologies and also due to their sub-nanosecond response time and high light sensitivity [1]. SPAD devices are frequently used for several purposes: Time-Of-Flight (TOF) [2] for 3D imaging and LIDAR applications, charged particle detection for medical and high energy physics applications [3], Fluorescence Lifetime Imaging Microscopy (FLIM) for biological applications [4]. SPAD devices have been implemented in 28nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology, which allows intrinsic 3D pixel [5] and indirect sensing of SPAD avalanche events [6]. In this technology, SPAD devices are implemented below the buried oxide (BOX) layer and the electronic logic circuits are inserted in the thin silicon layer on top of the BOX layer, which provides an intrinsic 3D stack and a much higher fill-factor.

One of the key figures of merit of SPAD devices is the Photon Detection Probability (PDP) leading to important research studies. PDP represents the SPAD devices' sensitivity and is defined as the probability of an absorbed incident photon to generate an avalanche event. PDP is affected by several factors: wavelength, applied voltage, photogeneration rate, electric field, doping levels. In order to improve the PDP, authors in [7]-[9] respectively employ the following approaches: i) an optimized SPAD architecture with charge-focusing, ii) an increase of light-material interaction thanks to nanostructuration, and iii) a germanium cavity as an absorption layer. In this study, we propose an efficient 3D electro-optical simulation method to estimate the PDP. Then, using the proposed electro-optical simulation flow, we implement the light-trapping approach to improve the PDP of SPAD devices implemented in 28nm FD-SOI CMOS technology.

The method to optimize the PDP uses a simulation flow described in section II where the electrical behaviour of SPAD structure is also considered. In section III, the simulation methodology with the light-trapping approach is presented. Simulation results of proposed electro-optical simulation flow are reported and discussed in section IV.

II. PHOTON DETECTION PROBABILY SIMULATION METHOD

In order to estimate the PDP of SPAD devices, we integrated the product of the Avalanche Triggering Probability (ATP) and the electron-hole photogeneration rate (G) over the active volume (V) of the SPAD. Then we divided by the incident photon flux $\Phi_{photons}$(number per second) at the considered wavelength λ:

$$PDP(\lambda) = \frac{1}{\Phi_{photons}(\lambda)} \iiint ATP(x,y,z) * G(x,y,z,\lambda) dV \quad (1)$$

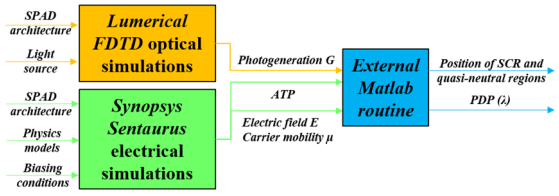

Figure 1 Block diagram of Photon Detection Probability estimation

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The simulation flow was then divided into two parts: electrical part and optical part. We performed the electrical and optical simulations with *Synopsys Sentaurus* and *Lumerical FDTD* respectively to obtain data for both the electrical data (ATP, electric field E, carrier mobility μ) and optical data (photogeneration rate G). Data are combined and postprocessed within an external *Matlab* routine, as shown in Fig. 1.

We considered that the SPAD was composed of the Space Charge Region – SCR (as multiplication region) and two quasi-neutral regions, one p-type doped on top of the SCR and the other n-type doped at the bottom of the SCR. We calculated the limits of the active region (where photogenerated carriers effectively lead to an avalanche event) by investigating the electric field distribution across the structure and also the ratio of drift and diffusion velocities of minority carriers in each quasi-neutral region to consider the contribution of these regions to the PDP. Fig. 2 and 3 illustrate the profiles of electric field and ratio of drift and diffusion velocities of minority carriers respectively at the p-side and the n-side limits of SCR with an excess voltage of 1.5V (15% of the breakdown voltage).

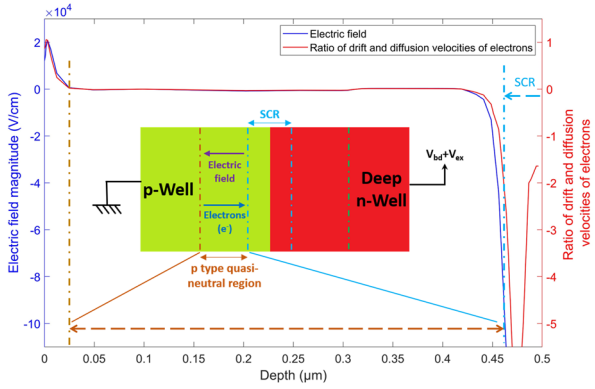

Figure 2 Profiles of electric filed and ratio of drift and diffusion velocities of electrons at the p-side limit of SCR

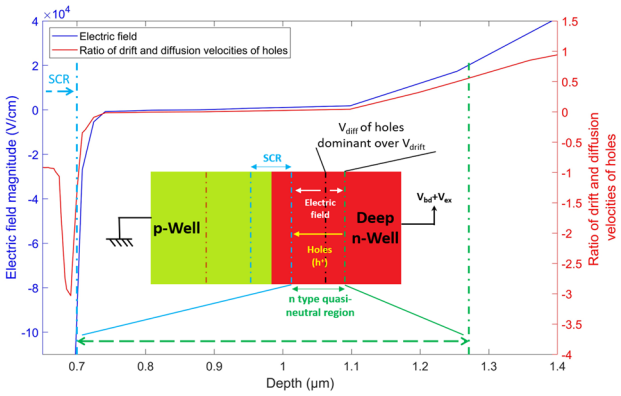

Figure 3 Profiles of electric filed and ratio of drift and diffusion velocities of holes at the n-side limit of SCR

We considered that the beginning of p-type quasi-neutral region was given by the direction of electrical field that was favourable for electrons and the beginning of SCR (end of p-type quasi-neutral region) corresponded to the position where the electric field magnitude was below the threshold of -10^5V/cm. The end of SCR (beginning of n-type quasi-neutral region) was where the electric filed surpassed the threshold. For the end of the n-type quasi-neutral region, the diffusion velocity (V_{diff})of holes is dominant over the drift velocity (V_{drift}) of holes in some areas and we considered that when the ratio V_{drift}/V_{diff} was above 0.5, the n-type quasi-neutral region ended.

The electrical simulations were 2D cylindrical symmetry whereas the optical simulations were 3D (with adapted limit conditions linked to spatial period). The external *Matlab* routine was able to extrapolate the 2D electrical data according to the cylindrical symmetry and to create 3D matrix of electrical data. It was thus able to combine 2D electrical and 3D optical data to calculate the PDP.

III. Simulation Methodology

A cross section of the investigated SPAD implemented in 28nm FD-SOI CMOS technology is shown in Fig. 4. In the active region above the p-Well, design rules dictate the existence of Shallow Trench Isolation (STI) between silicon regions. We artificially used these blocks of STI properly choosing their dimensions and positions, to realize a photonic crystal layer (diffraction grating) providing light-trapping effects, in order to locate the maximum of interferences in the SCR.

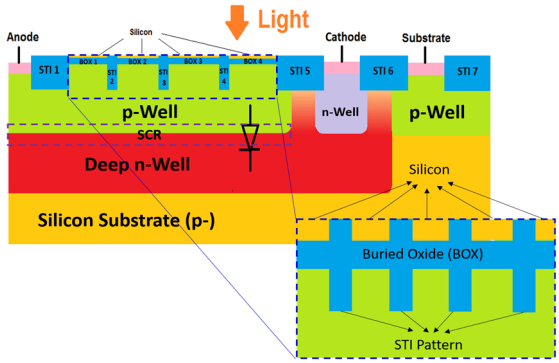

Figure 4 Schematic of SPAD implemented in 28nm FD-SOI CMOS technology (Scales are not respected and BEOL layers are not represented)

From the optical point of view, the SPAD structure could be simplified as shown in Fig. 5. Here the SiO_2 region and silicon substrate region are considered semi-infinite.

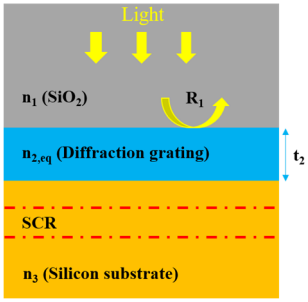

Figure 5 Simplified equivalent optical schematic of the SPAD structure

The problematic of improving the photon detection efficiency with a diffraction grating comes down to maximizing the light intensity in the SCR (multiplication region). This optimisation is thus realised in two steps. Firstly, the pattern plays the role of an antireflection coating in the case of Front-Side Illumination (FSI) to minimize the reflection coefficient R_1 at interface SiO_2/diffraction grating. R_1 is function of the optical index n_1, n_2 and n_3 and the diffraction grating thickness t_2. The

equivalent optical refractive index $n_{2,eq}$ in the case of FSI follows an effective medium law [10]:

$$n_{2,eq}^2 = n_{SiO_2}^2 * (1 - FF) + n_{silicon}^2 * FF \quad (2)$$

Here the Filling Factor (FF) is defined as the ratio between the silicon area and the total area of one pattern with square shape. The equivalent optical index of diffraction grating layer is thus function of FF. The second step consists of using the interferences of diffraction grating to locate the maximum of light intensity in the SCR where the ATP is the highest. The position of the maximums of interferences is function of the pattern period. Suitable pattern periods allow to improve the photogeneration rate in the SCR and thus to improve the general photon detection probability.

Our simulation methodology is to first find the optimal FF of STI which allows the maximum light transmission by performing optical simulations with a small pattern period (less than 100nm). Once the optimal FF is found, the second step is to extract the optimal spatial period allowing the constructive interferences in the SCR.

IV. Simulation Results

The simulation methodology was applied to SPAD implemented in 28nm FD-SOI CMOS technology (Fig. 4) in the case of FSI with several constrains. The first one is that the depth of STI blocks is fixed by the technological process. Additionally, the process design rules impose certain restrictions on width, length of STI areas and distance between them. As the SPAD devices are fabricated in standard process, the second constraint refers to Back-end-of-Line (BEOL) layers, which are not optimized for optical light transmission (moreover, their optical properties are not fully characterized). Nevertheless, the optimisation strategy still remains effective.

In the first step, several values of FF were simulated at wavelengths of 500nm and 650nm. Fig. 6 and Fig. 7 respectively represent the profiles of electric field magnitude and photogeneration rate with FF = 0.15 at wavelength of 500nm and with a pattern period of 10nm. These profiles were extracted near the centre of one pattern and the incident light power was set to 1W/m². The curves showed a significant antireflection effect of pattern with different values of FF compared to reference structure, with a relative improvement of

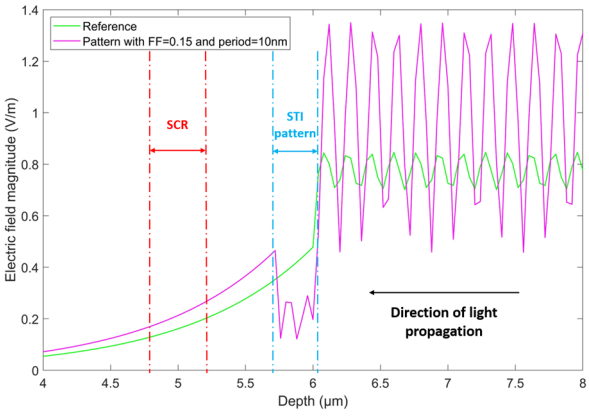

Figure 6 Profiles of electric field magnitude of reference SPAD and patterned SPAD with FF=0.15 and period=10nm

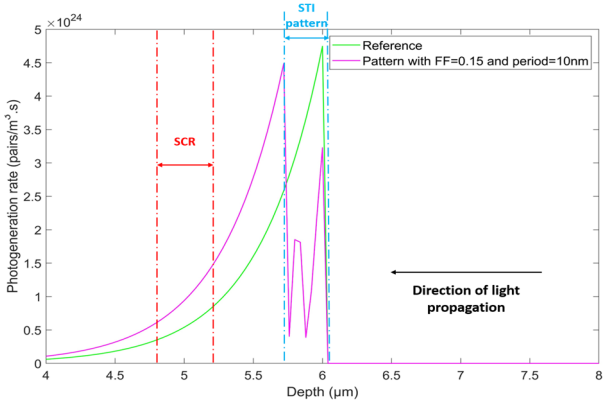

Figure 7 Profiles of photogeneration rate of reference SPAD and patterned SPAD with FF=0.15 and period=10nm

electric field magnitude up to 30% and of photogeneration rate up to 60%. Considering we didn't fully control the pattern dimensions, the antireflection effect could have been more significant.

The second step was dedicated to the optimisation of pattern period in order to locate the maximums of interferences in the SCR. Several values of pattern period for each FF were performed in simulations. Fig. 8 illustrates a cartography of photogeneration rate at wavelength of 500nm with a pattern period of 0.48µm and

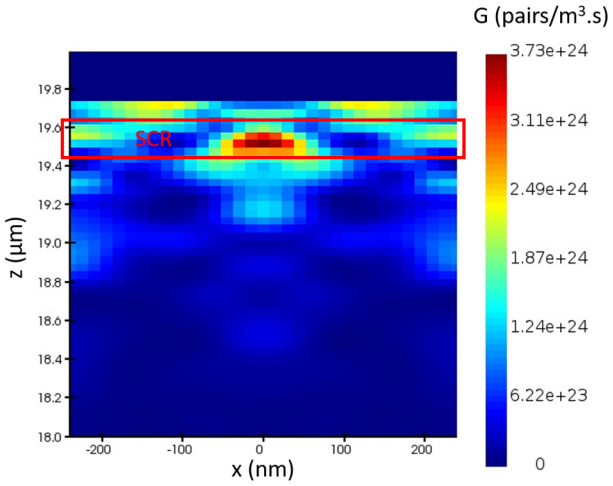

Figure 8 Cartography of photogeneration rate of patterned SPAD with FF=0.15 and period=0.48µm

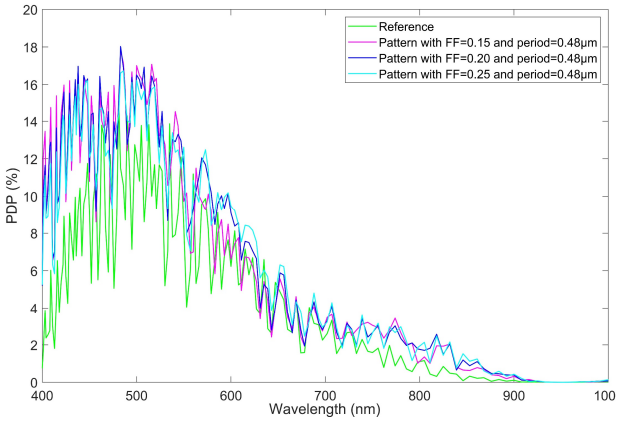

Figure 9 PDP Profiles of reference SPAD and patterned SPAD with excess voltage V_{ex}=0.6V

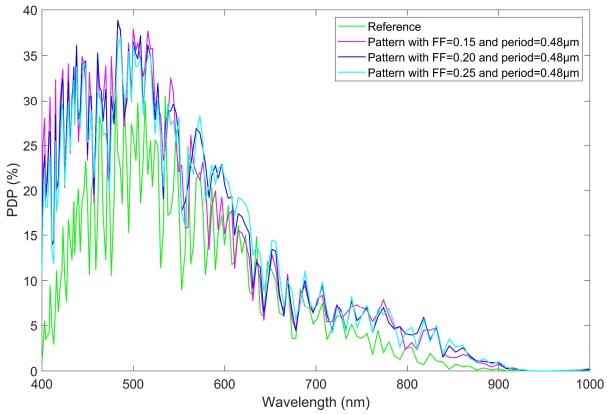

Figure 10 PDP Profiles of reference SPAD and patterned SPAD with excess voltage V_{ex}=1.5V

an FF of 0.15. The SCR was located 180nm away from the interface diffraction grating/silicon substrate. We could observe the presence of a hot spot in the SCR, showing clearly the diffracting effect of the pattern.

These period dimensions were then used in the simulations with a larger range of wavelengths of 400-1000nm in order to investigate the improvement for other wavelengths. Fig. 9 and Fig. 10 respectively illustrate the PDP profiles with an excess voltage V_{ex} of 0.6V and 1.5V (respectively excess of 6% and 15% of the breakdown voltage V_{bd}). The second value of V_{ex} allows higher values of ATP and consequently of PDP, thus greater difference between patterning SPAD and reference SPAD. The curves show a clear relative improvement of the PDP for shorter and longer wavelengths. For mid-range wavelengths, the gain in PDP is relatively smaller with higher absolute values of PDP though. The relative gain could reach 700% at specific wavelengths and the average relative gain could reach over 100% in the considered range of wavelengths.

Thanks to these simulation results, we have submitted three pattern dimensions for IC fabrication and for future characterization. Table I summarizes the simulated relative improvement of the submitted patterns in different ranges of wavelengths.

Table 1 Simulated relative gain of submitted pattern compared to reference SPAD

FF	Pattern period (µm)	Average relative gain compared to reference
0.15	0.48	400nm < λ < 550nm: ~ 140%
		550nm < λ < 750nm: ~ 25%
		750nm < λ <1000nm: ~ 250%
0.20	0.48	400nm < λ < 550nm: ~ 130%
		550nm < λ < 750nm: ~ 30%
		750nm < λ <1000nm: ~ 340%
0.25	0.48	400nm < λ < 550nm: ~ 110%
		550nm < λ < 750nm: ~ 40%
		750nm < λ <1000nm: ~ 380%

V. CONCLUSION

In this article, a 3D electro-optical simulation method for SPAD Photon Detection Probability (PDP) calculation is presented. Then light-trapping concept thanks to the patterning of STI layer is proposed to improve the PDP of a SPAD fabricated in 28nm FD-SOI CMOS technology (with Front Side Illumination). The maximum relative gain of 700% was reached at specific wavelengths and an average gain of 100% in the range of wavelengths of 400-1000nm was also obtained. These encouraging results have permitted IC fabrication including several designs of FD-SOI CMOS SPADs with different STI pattern sizes. Future work will address the characterization of samples with/without an STI pattern and improving the PDP in the case of Back-Side Illumination.

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