Potential Engineering to Enhance Transfer Characteristics of Advanced CIS Pixel based on VTG - FDTI scheme

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***Abstract*— The transfer characteristics of the three different CMOS image sensor (CIS) pixel schemes; the vertical transfer gate (VTG) with the front-side deep trench isolation (FDTI), the VTG with the back-side deep trench isolation (BDTI), and the planar transfer gate (PTG) with the BDTI are rigorously studied with 3D TCAD simulation. The electrical potential profiles of photo-diode (PD) region are optimized in terms of full well capacity (FWC) and transfer characteristics for each scheme. The simulated blooming margin potentials are well matched to the experimental blooming signal. According to our TCAD analysis, the VTG with the FDTI scheme showed high full FWC characteristics compared to the PTG with the BDTI and the VTG with the BDTI.**

Keywords—CMOS Image Sensor, Pixel Scaling, Small Pixel, SNR, Crosstalk, Blooming, Deep Trench Isolation, Transfer Gate.

I. INTRODUCTION

Recently, various CIS pixel schemes have been actively investigated to scale down pixel size to sub-micrometers to achieve higher resolution for mobile and automotive applications [1]. As the pitch size of the pixel decreases, serious deterioration of signal-to-noise ratio (SNR) can be caused by degradation of the sensor sensitivity. While the sensitivity issue can be overcome with new optical schemes, such as Tetracell, Nonacell, and 2x2 on-chip lens [2], maintaining high FWC and small crosstalk in smaller pixels is challenging in terms of resolution enhancement. According to recent researches, three types of unit pixel schemes have been mainly presented. The first one is the unit pixel with conventional PTG based on the BDTI process, as shown in Fig. 1 (a) [3]. The second and third pixel schemes have common VTG structures, as shown in Fig.1 (b) and (c) [4], where the VTG structure is fabricated with BDTI (b), and the VTG structure is built on the FDTI process (c), respectively [5]. In this work, we analyzed 0.6x um pixels and performed the process and the device simulations for a unit pixel domain consisting of PD and transfer gate (TG), as shown in Fig. 2 with in-house 3-D TCAD simulation tool. Also, we compared the electrical properties of the three different unit pixel schemes in terms of FWC, transfer characteristics, and blooming. For fair comparison, we carefully optimized the implantation conditions to achieve the best electrical properties for each pixel scheme. We expect that this analysis would provide a valuable intuition for further optimization of various pixels in sub-micron scale.

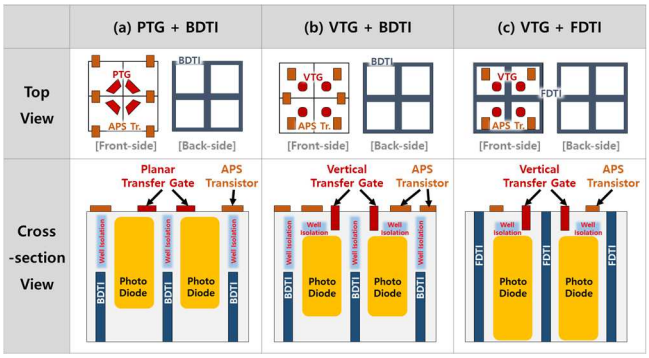

Fig. 1. Unit pixel schemes: (a) PTG with BDTI, (b) VTG with BDTI and (c) VTG with FDTI.

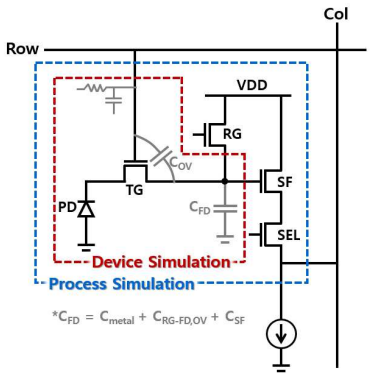

Fig. 2. The circuit schematic of a unit pixel and the domain of TCAD simulation.

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II. Pixel Schemes in CMOS Image Sensor

First, we will explain about the TG design. Especially, the structure of the TG is important not only in terms of transferring electrons from the PD to the floating diffusion (FD) area, but also efficient design of the transistors that make up the unit pixels (source follower amplifier, reset and select transistors). In the case of the PTG scheme, the transistors in a unit pixel should only be placed in the pixel edge region for the prevention of the punch-through between the transistors and the PD, as shown in Fig. 1 (a). In the VTG scheme, the transistors can be fabricated on the silicon surface area regardless of the specific position because the well isolation is formed to suppress the punch-thorough, as shown in Fig. 1 (b) and (c). So, it can provide efficient ways to overcome short-channel effects with high integration density. Next, the isolation processes among pixels in sub-micrometer scale region can be mainly categorized into the BDTI and FDTI types. While pixels with BDTI are partially isolated, pixels based on the FDTI process are completely blocked by the insulator.

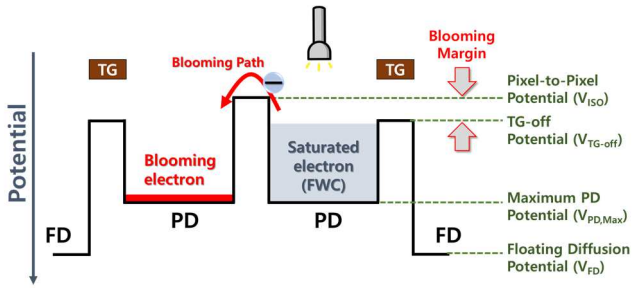

Fig. 3 The schematic of potential distribution under the shutter-off (TG-off) condition.

Fig. 3 illustrates the schematic of the potential distribution under the shutter-off condition (TG-off operation). The blooming margin is presented by the difference between the pixel-to-pixel potential (V_{ISO}) and TG-off potential (V_{TG-off}) (Eq. 1). The blooming is caused by excess photo-carriers spilled into adjacent pixels under over-saturated conditions [6]. The FWC is calculated by integration of electrons in the PD (Eq. 2). In addition, the FWC is proportional to the difference between the maximum PD potential ($V_{PD,max}$) and V_{TG-off}.

$$Blooming\ Margin = V_{TG-off} - V_{ISO} \quad \text{(Eq. 1)}$$

$$FWC = \int^{PD} Q dv = \frac{1}{q}\int^{PD} C_{PD} V_{PD} dv$$
$$, \text{where } V_{PD} = V_{PD,Max} - V_{TG-off} \quad \text{(Eq. 2)}$$

To obtain high FWC, the PD should be designed to have as high $V_{PD,max}$ as possible, which requires high TG-on bias since PD should be fully depleted at the shutter operation. Plus, V_{TG-off} should be controlled with a low value. However, this decreases blooming margin. In this analysis, the simulated pixels were optimized taking into account with the relation between blooming and the FWC.

III. Result & Discussion

In Fig. 4, we show model-to-hardware correlation of the measured blooming signals via blooming margin potential extracted from TCAD simulation. The sample is fabricated with the PTG and BDTI. The measured blooming signal increases steeply below 500 mV. This result indicates that the simulation results on blooming margin are strongly correlated with the blooming signals

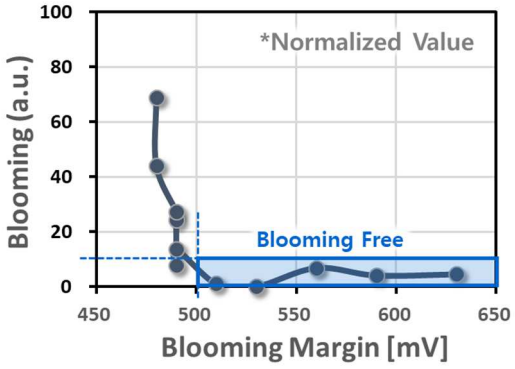

Fig. 4. Correlations between the measured blooming and the blooming margin potential obtained from simulation.

Fig. 5 shows the equi-doping concentration surface of the three different pixel schemes, where the implantation conditions are optimized in terms of the blooming margin, the FWC, and the transfer characteristics.

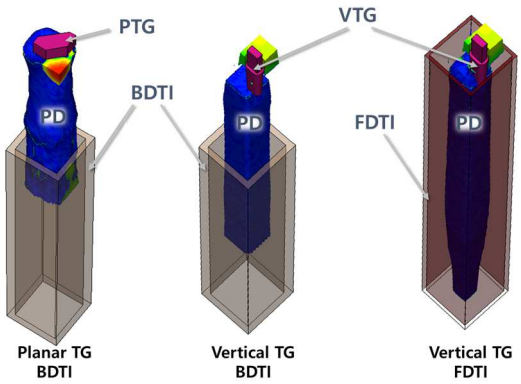

Fig. 5. The equal-doping concentration surface of the three different pixel schemes.

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Fig. 6 shows the signal response according to the exposure time, where the saturated signal means the FWC. Although $V_{PD,max}$ of the BDTI scheme is higher than that of the FDTI scheme, as shown in the "B region" of Fig. 7, the FWC is remarkably low, as shown in Fig. 6. In addition, the pixel based on the FDTI process has the extended PD compared to conventional processes, as shown in Fig. 5 and Fig. 7. Since the blooming margin in the FDTI scheme need not be considered, $V_{TG\text{-}off}$ can be designed with a very low value. The blooming margins are 600 mV in the PTG with BDTI, 550 mV in the VTG with BDTI, and infinite in the VTG with FDTI schemes. These results show that the VTG scheme based the FDTI process is most suitable to enhance the FWC characteristics.

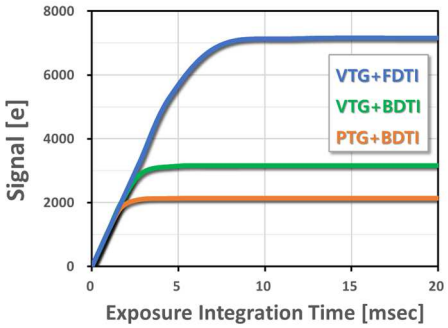

Fig. 6. The signal response according to the exposure integration time.

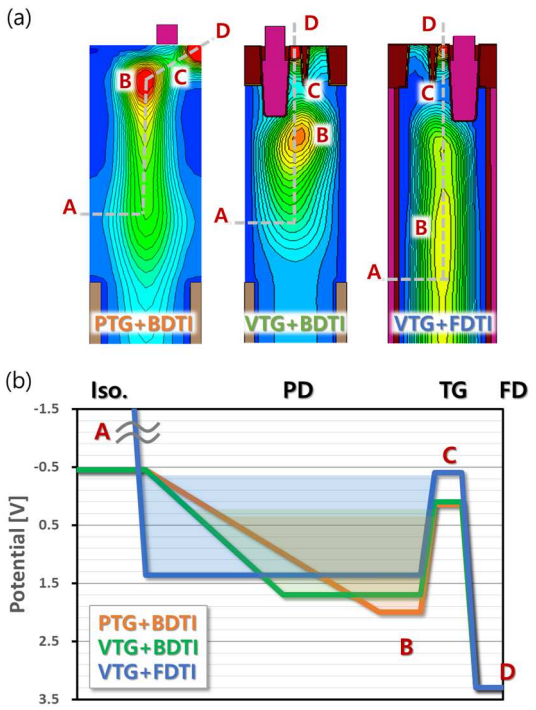

Fig. 7. The depth dependent 2-D potential profiles (a) and 1-D potential schematic curves (b) of three pixel schemes under TG-off.

Figure 8 shows the residual characteristics as a function of TG-on bias, where y-axis indicates the amount of residual electrons in the PD after shutter operation. As the TG-on bias increases, the residual electrons markedly decline. When the residual electrons are present, noise image appears prominently under low illumination. In addition, the enhancement of residual characteristics affects the improvement of the shutter speed. While the TG-on bias voltage should be higher than 2.8 V to obtain zero residual condition for the pixel scheme with the BDTI and the PTG, residual electrons disappear beyond 1.6 V of the TG bias voltage in the case of the pixel scheme with the FDTI and the VTG.

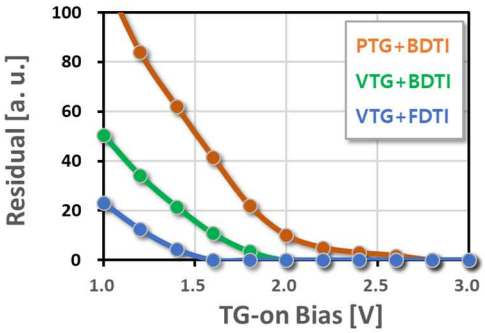

Fig. 8. The comparison of the residual characteristics as a function of TG-on bias in various types of unit pixel.

Fig. 9 shows the 1-D electrical potential curves from the PD to the FD node under TG-on operation. These results indicate the transfer potential barrier in the VTG with FDTI scheme is lower than that of the other two schemes at TG-on bias of 1.6V.

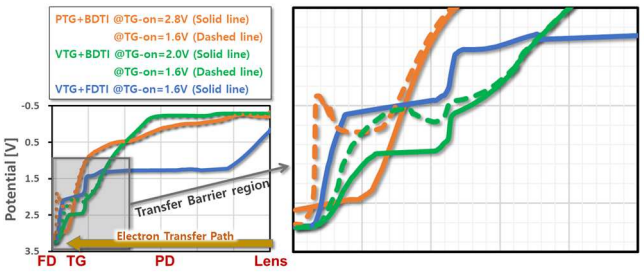

Fig. 9. The depth dependent 1-D potential curves of three pixel schemes under TG-on.

In conclusion, through the comprehensive analysis of the potential distribution, the VTG based on the FDTI process is considered more useful in designing sub-micron scale pixels compared to other types of structures in terms of efficient transfer and high FWC characteristics. We summarized the overall electrical properties of the three different unit pixels through TCAD analysis in Table 1, where pixels with 0.6x um pitch are used for the analysis.

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Table 1. The electrical properties of three different unit pixels.

Type	PTG + BDTI	VTG + BDTI	VTG + FDTI
Full Well Capacity	2000e-	3000e-	7000e-
Residual Electron @ TG Bias = 1.8V	20e-	5e-	Free
TG Bias @ Residual is free	2.8V	2.0V	1.6V
Maximum PD Potential	2.0V	1.7V	1.3V
Blooming Margin	600mV	550mV	X

IV. CONCLUSION

In summary, we have investigated the crucial electrical properties of three different pixel schemes via full 3D TCAD simulation. The results show that the VTG with FDTI scheme has higher FWC and better transfer characteristics than the other two pixel schemes (PTG/VTG with BDTI). We believe that this work presents a useful insight for the new pixel schemes in sub-micrometer scale.

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