Modeling of Doping Effects in Surface Potential Based Compact Model of Fully Depleted SOI MOSFET

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***Abstract*— The Fully-Depleted Silicon On Insulator (FDSOI) technologies are deployed for a wide range of applications (digital, analog, RF, etc.) requiring a large variety of MOS transistors. These transistors are defined by several dedicated specificities such as their threshold voltage or their gate oxide thickness. Usually, the surface potential (SP) based compact model of FDSOI MOSFET supposes an undoped channel with metal gate in front and back contact [1-3]. These models are not sufficiently accurate for real devices; thus, in the modern compact models [1-3], a lot of parasitic effects must be included such as the substrate depletion. This paper describes the recent improvements of L-UTSOI standard model, with the introduction of the poly-depletion effect and an enhanced model of the substrate doping effects. These model extensions are validated against silicon experimental data and available in the latest official model release.**

Keywords— L-UTSOI, compact model, SPICE, FDSOI.

I. INTRODUCTION

L-UTSOI is standard SPICE model [1] dedicated to FDSOI Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) technologies. All relevant physical effects such as mobility degradation at high field, velocity saturation, short channel effects, gate currents, backplane depletion, gate induced source/drain leakage, STI induced stress effects, self-heating, etc are included [3-4]. L-UTSOI model gives an accurate description of currents, charges and their derivatives (i.e. transconductance, conductance and capacitances and higher order derivatives).

As explained in previous papers [3-4], L-UTSOI is the first available standard compact model able to describe the behavior of an ultra-thin body and BOX FDSOI MOSFET in all bias configurations including the strongly inverted back interface effect. Thus, an original analytical calculation routine based on Poisson's equation considering only mobile charges (i.e. electron in NMOS case) has beens developed to compute the values of the surface potentials at front and back interfaces in all operating conditions as detailed in [3-4]. Nevertheless, in usual FDSOI MOSFET, three parts of the device can be intentionally doped to control the threshold voltage in different transistor

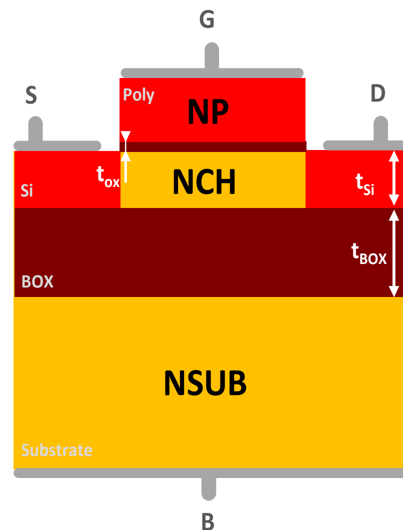

Fig. 1: FDSOI structure and definition of the main geometrical, doping and electrical parameters. NCH is doping in channel; NSUB is doping in substrate; NP is doping in polysilicon gate; y is the position perpendicular to SiO2/Si interface.

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flavors: the substrate, the channel and the gate by using doped polysilicon (respectively labelled NSUB, NCH and NP for the doping values as illustrated schematically on Fig. 1). The modeling of the channel doping (NCH), was previously included through a corresponding flat-band voltage shift VFB on front and back interfaces (validated for N-type and P-type doping from undoped to few 10^{18} cm^{-3}); more details are available in the documentation [3]. Such doping effect is generally challenging to implement in present compact model because a rigorous approach would require rebuilding analytical Poisson's equation including new boundary condition. Another way is to find a corrective solution to the core model to describe the first order effect.

In this paper, we present the new physical insights included in L-UTSOI model version 102.5 [3] relative to doping effect. In Section II, we focus on the improvement of substrate depletion to perfectly describe CGB-CBG capacitance & reciprocal capacitance for low substrate doping and high VGS value, in section III, we describe the introduction of new Poly-Depletion model.

II. Enhanced Model of Substrate Doping Effects: Impact of the Back Channel Inversion

The substrate depletion effect (i.e. NSUB) was originally introduced in the model as a boundary condition based on dedicated calculation of the substrate/BOX interface potential (inspired from the SP routine in PSP model [5]) prior to main channel SP calculation. For that, the assumption is to consider the gate oxide - silicon film - BOX stack (the part between the substrate and the gate) as a unique perfect dielectric and to ignore the presence of mobile carriers in the channel. This approach allows obtaining a compact model able to describe accurately the substrate depletion effect on the currents and most of the capacitances.

Unfortunately, this approach leads to unphysical CGB behavior in inversion where CGB decreases more than expected because we ignore the back channel inversion. The corrective solution is to replace the gate voltage by an approximated back channel surface potential using a similar initial guess for back surface potential as the core model [3-4].

Fig. 2 (2.a potential at the substrate/BOX and 2.b CGB capacitance) illustrates the model behavior in different configurations. Plain black curve is without substrate depletion, blue dotted curve is the case where the gate oxide - silicon film - BOX stack is an equivalent dielectric and plain red curve is the case where the back channel inversion is included. As the red curve shows, accounting for the back channel inversion drastically improves the CGB description.

Finally, this is confirmed on Fig. 3 (3.a to3. d) where the model agreement with experimental data from a 28nm FD-SOI technology is shown for both CGB and CBG (3.c & 3.d), among others capacitances and reciprocal capacitances characteristic of such device.

III. Modeling of Poly-Depletion Effect

L-UTSOI model is initially optimized for advanced technologies using High-K - metal gate; moreover, it can be used for technologies using polysilicon gate by the addition of

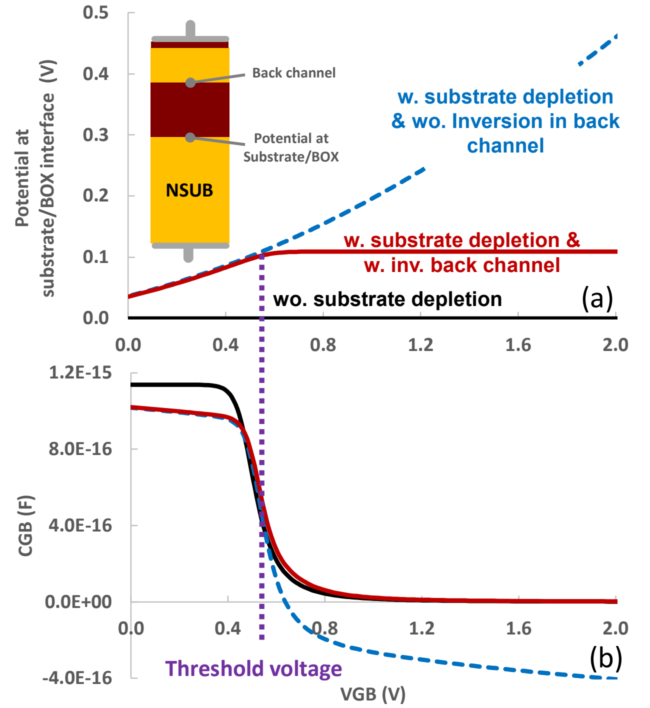

Fig. 2: Model in different configuration: For long & wide device with t_{ox}=2nm, t_{Si}=10nm, t_{BOX}=25nm and NSUB=5e17 cm^{-3} p doping. (a) Potential at substrate/BOX interface and (b) CGB capacitance versus VGS with VBS=VDS=0 without and with substrate depletion including or not inversion in back channel.

the well-known Poly-Depletion effect due to the gate doping. To model this effect we propose a corrective factor that approximates the Poly-Depleted gate charge.

Starting from classical Poisson's equation in the polysilicon gate:

$$\frac{d^2\Psi}{dy^2} = \frac{q}{\varepsilon_{si}}\left(N_p - N_p.e^{-\frac{\Psi}{ut}}\right) \quad (1)$$

and after integration using boundary conditions (electric field far from SiO_2/silicon interface is set to 0):

$$\frac{1}{2}\cdot\left(\frac{d\Psi_p}{dy}\right)^2 = \frac{q.N_p}{\varepsilon_{si}}\left(\Psi_p + ut.e^{-\frac{\Psi_p}{ut}} - ut\right) \approx \frac{q.N_p}{\varepsilon_{si}}(\Psi_p) \quad (2)$$

where Ψ is the y position dependent potential; Ψ_p is the surface potential at the SiO_2/Polysilicon interface; ; Ψ_s is the surface potential at the SiO_2/silicon interface; ε_{si} is the dielectric permittivity of silicon; q is the electron charge; ut is the thermal voltage and N_p is the polysilicon doping. Note that the simplification is justified by the fact that the gate is indeed depleted when we have inversion regime in the channel; thus in this case the surface potentials (at SiO_2/Polysilicon and SiO_2/silicon interfaces) are positive.

Then, the normalized Poly-Depleted charge is:

$$q_{g,pd} = kp.\sqrt{\Psi_p} \quad (3)$$

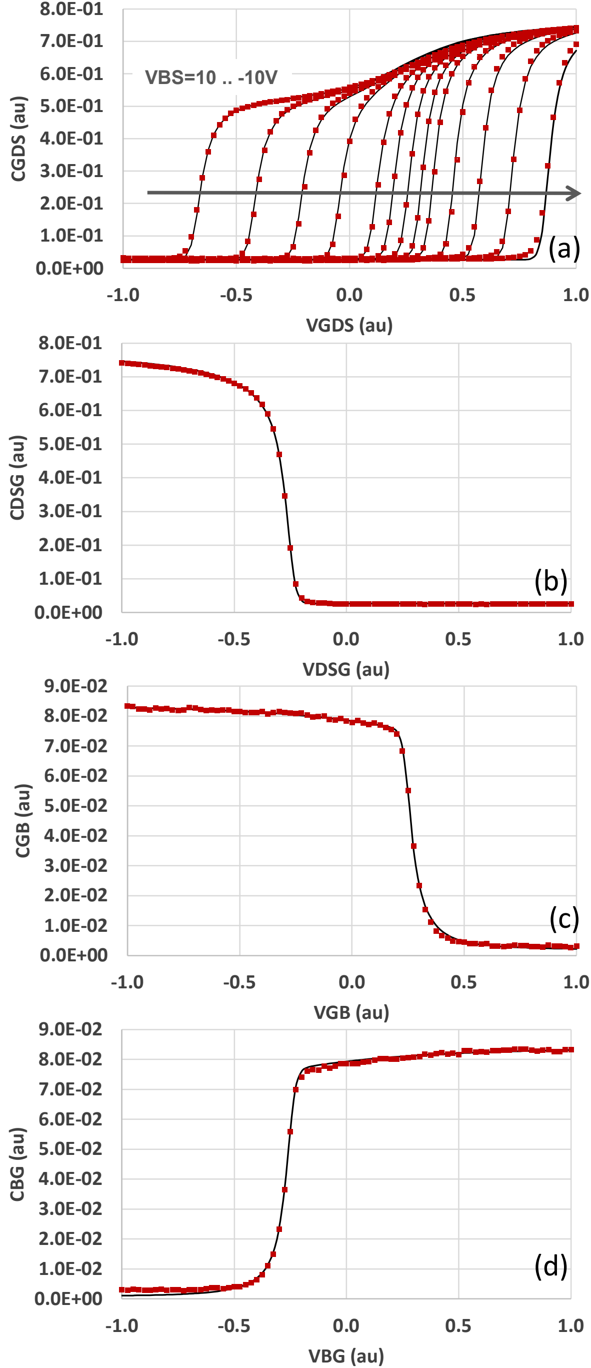

Fig. 3: Comparison between measurement from 28nm technology (symbol) and model including improvement on substrate depletion (line): For long & wide device. (a) CGDS (high node on G and low node on DS) versus VGDS at different VBS, (b) CDSG (high node on DS and low node on G) versus VDSG, (c) CGB (high node on G and low node on B) versus VGB and (d) CBG (high node on B and low node on G) versus VBG.

where $q_{g,pd}$ is the gate charge including Poly-Depletion normalized to C_{ox}; kp is equal to $\sqrt{2.q.\varepsilon_{si}.N_p}/C_{ox}$ and C_{ox} is the front gate oxide. This charge being equal to the charge across the gate oxide capacitance, we obtain the formulation of Ψ_p as in [6]:

$$C_{ox}.\left(V_{GS}-\Psi_s-\Psi_p\right)=kp.C_{ox}.\sqrt{\Psi_p} \quad (4.a)$$

$$\Psi_p=\left(\sqrt{\left(V_{GS}-\Psi_s\right)+\frac{kp^2}{4}}-\frac{kp}{2}\right)^2 \quad (4.b)$$

This last equation is implicit because Ψ_s is interdependent with Ψ_p. However, as explained earlier, our objective is to find a corrective factor of Poly-Depletion defined by the ratio between the charge with and without Poly-Depletion, in which $q_{g,0}=\left(V_{GS}-\Psi_s\right)$ is approximated by the calculation of surface potential without included Poly-Depletion effect:

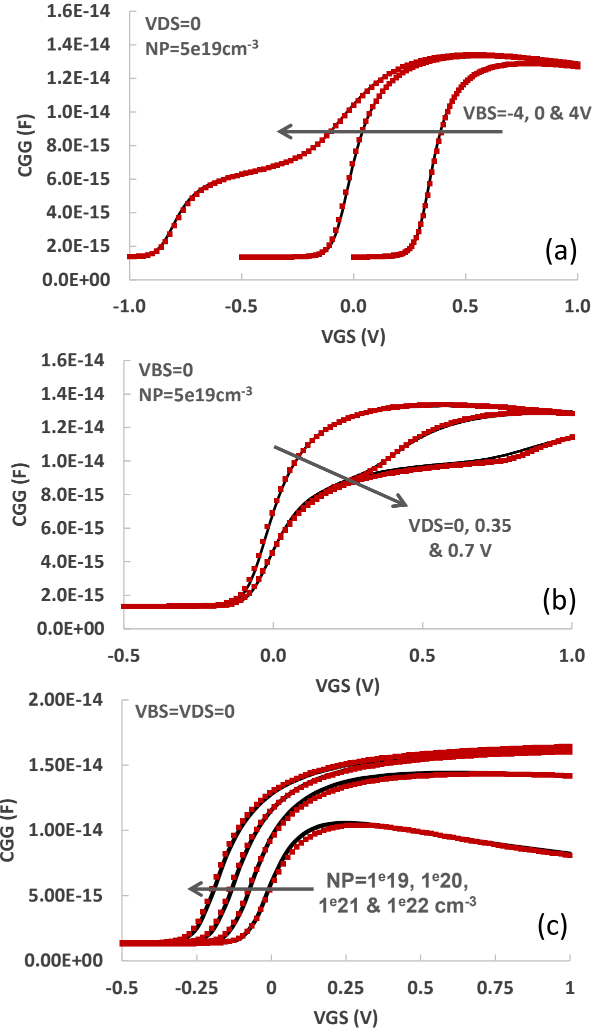

Fig. 4: Comparison between TCAD (symbol) and model including Poly-Depletion (line) for NMOS: For long & wide device with t_{ox}=2nm, t_{Si}=10n and t_{BOX}=25n. (a) CGG versus VGS at different VBS, (b) CGG versus VGS at different VDS for VBS=0 and (c) CGG versus VGS at different NP that illustrating model predictability.

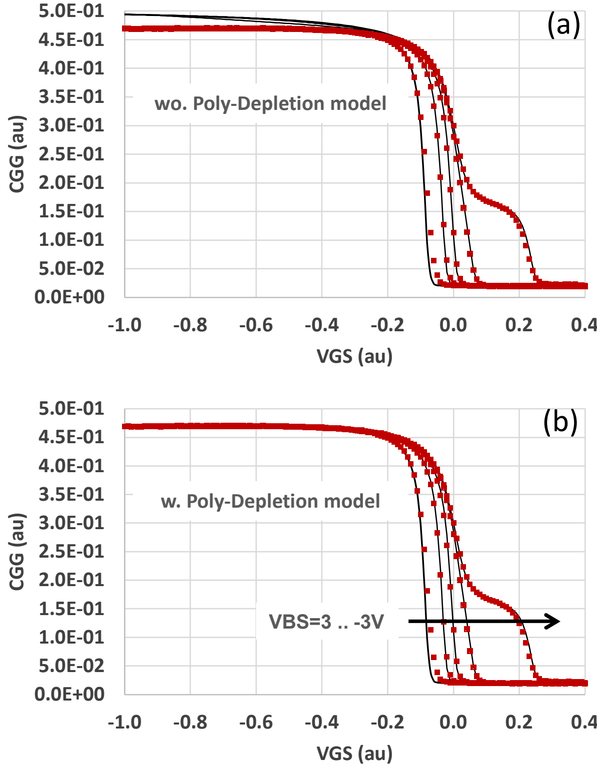

Fig. 5: Comparison between measurement from Qualcomm (symbol) and model including Poly-Depletion (line) for PMOS device: For long & wide device. (a) CGG versus VGS at different VBS without Poly-Depletion model, (b) CGG versus VGS at different VBS with Poly-Depletion model.

$$\mathrm{Ratio} = \frac{q_{g,pd}}{q_{g,0}} \approx 1 - \frac{\left(\sqrt{q_{g,0} + \frac{kp^2}{4}} - \frac{kp}{2}\right)^2}{q_{g,0}} \qquad (5)$$

At the end, this ratio is applied (as a corrective factor) to the current and the front gate charge. Moreover, to account for the flat band shift induced by the polysilicon gate, we add the value of $ut.\ln(NP/ni)$ to the flat-band voltage, which is an interesting feature for variability study. Finally, note that this approach is a "first order correction". For very low doping concentration in polysilicon (under 10^{19} cm^{-3}, which is outside usual process condition), the model accuracy is limited but remains reasonable anyway.

Fig. 4.a and 4.b show the good agreement with TCAD simulation [7] of the capacitances for various conditions, illustrating the well-reproduced drain-source partitioning over VDS (Fig. 4.b) despite the simplicity of this approach. Fig 4.c illustrates the model predictability when NP is varied as in TCAD simulations without any fitting parameter. Finally, Fig. 5 is the comparison on the total gate capacitance, evidencing the good agreement of the model with the experimental data.

IV. Conclusion

In this paper, we have presented the recent developments brought to L-UTSOI model to improve its accuracy and versatility in present technological usage. Firstly, the improvement of substrate depletion is essential to describe accurately the RF figure of merit in Quasi-Static condition where substrate doping is an important process parameter. Secondly, Poly-Depletion model proposed here through a corrective factor enlarges model capability to other gate process option like polysilicon gate.

Global runtime evaluation realized on ring-oscillator FanOut=3 shows an increase of runtime by 2-3% with substrate doping modification and <1% with Poly-Depletion model. This could be explained by the location of the modification inside the code, since recalculation of the substrate depletion arrives before surface potential calculation and ratio factor of Poly-Depletion effect is a posteriori correction. However, the penalty on the runtime remains minor.

The L-UTSOI model is available in all major commercial SPICE simulators. Those enhancements significantly contribute to demonstrate L-UTSOI readiness for circuit design applications dedicated to FDSOI device.

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