Equivalent Circuit Macro-Compact Model of the 1T Bipolar SRAM Cell

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***Abstract*—In this work we report the development of a macro-compact model of the one-transistor (1T) bipolar SRAM Cell based on an equivalent circuit representation. The compact model consists of a combination of MOSFET, BJT, and other passive components. We start with calibration of the TCAD deck using experimental data and realize the operation of the 1T SRAM cell. Then we calibrate the different components of the SPICE compact model using TCAD simulation results at the 28 nm technology node. Finally, we show a comparison of the full switching sequence obtained from TCAD and SPICE simulations demonstrating the validity of the compact model.**

***Index Terms*—1T-SRAM; TCAD; SPICE; Compact Model; Transient Simulation**

I. Introduction

A novel bi-stable, one transistor (1T) bipolar SRAM cell with a floating p-base has been previously reported [1], [2], which has the potential to massively reduce the SRAM real estate compared to the traditional 6T SRAM cell. The cell has been comprehensively studied experimentally as well as using using TCAD simulations [3]. In this paper for the first time, we present a physics-based equivalent circuit macro-compact model of the 1T SRAM Cell suitable for SPICE circuit simulations and verification. We use TCAD simulation data to generate the target current-voltage characteristics for the individual SPICE compact model components of the macro-model and carry out the compact model extraction. Certain limitations of the selected component compact models are compensated by including additional circuit elements. We demonstrate the full operation of the 1T SRAM cell based on SPICE circuit simulations and perform a one-to-one comparison with the TCAD simulations.

II. 1T SRAM Cell Operation

In order to understand the role of the individual macro-circuit model components, in this section we first describe the structure and the operation of the 1T SRAM cell using TCAD simulations. The operation of the cell is based on an ion-implanted buried n-well 'boost' region, that leads to the creation of a floating p-well above it. More detailed description of the cell and physical analysis of its operation can be found in [3]. Fig. 1 illustrates the structure of the 1T SRAM cell obtained from Sentaurus process [4] simulations.

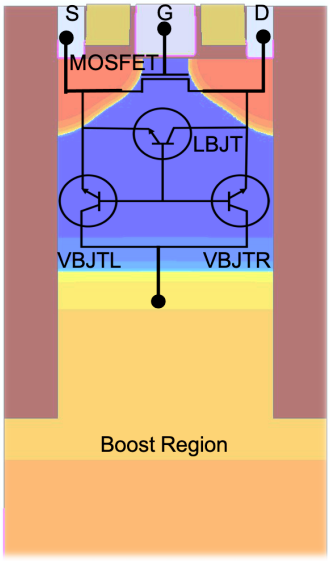

Fig. 1. The 1T SRAM cell structure (28 nm bulk CMOS technology) with an overlay showing the different built-in transistors. VBJTL and VBJTR are the left and right vertical BJTs, and LBJT refers to the lateral BJT.

The description of the cell operation states and the corresponding operating conditions are described below which have also been summarised in Table I:

HOLD '0' - no holes are stored in the floating p-region. The current is the MOSFET leakage current.
READ '0' - no holes are stored in the floating p-region. The current is the MOSFET current at V_G=0.7V, V_D=0.2V.
WRITE '1' - Impact ionisation hole current charges the floating p-region, reducing the built-in potential and turning on the BJTs.
HOLD '1' - The recombination of extra hole in the floating p-region is compensated by impact ionisation in the boost depletion region, keeping the built-in potential reduced.
READ '1' - The drain current is higher than the READ '0' current due to the forward biasing of the MOSFET substrate

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and the additional current of the lateral BJT.

First, the Sentaurus Device [5] TCAD simulations are meticulously calibrated against the MOSFET's experimental current-voltage characteristics. Then, to obtain the TCAD parameters that ensure an operational cell, we have conducted several design of experiments considering the impact of the two of the most critical physical models: Okuto impact ionization model [5], [6], and the concentration dependent SRH recombination model [5]. The key calibration parameters were b and $\tau_{\max}$ for Okuto and SRH models respectively. Fig. 2 illustrates the READ '0' and READ '1' current simulations in comparison with experimental data for different combination of the two parameters b and $\tau_{\max}$. The optimal combination is the one that guarantees full operation described above along with reasonably close values of the simulated READ currents to the experimentally observed ones.

TABLE I
1T-SRAM CELL OPERATION CONDITIONS

Cell Operation	Source Voltage (V)	Gate Voltage (V)	Drain Voltage (V)	Boost Voltage (V)
HOLD '0'	0	0.0	0.0	2
READ '0'	0	0.7	0.2	2
WRITE '1'	0	1.0	1.0	2
HOLD '1'	0	0.0	0.0	2
READ '1'	0	0.7	0.2	2

The potential distribution in the 1T SRAM cell during HOLD '0' and HOLD '1' is illustrated in Fig. 3 (a) and (b) respectively. As expected, the potential in the floating region increases during the HOLD '1'.

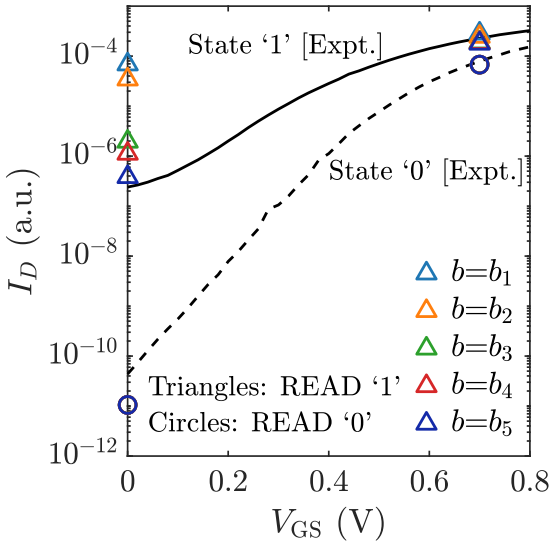


Fig. 2. Dependence of READ '0' and READ '1' currents on parameter b at a fixed $\tau_{\max}$ with $b_1 < b_2 < b_3 < b_4 < b_5$. The experimental curves are obtained by performing READ operations on the cell using different values of the gate voltage, considering the two states of cell - state '0' and state '1'. We have shown TCAD results for only two gate voltages of 0V and 0.7V. The drain voltage used for READ was fixed to V_D=0.2V.

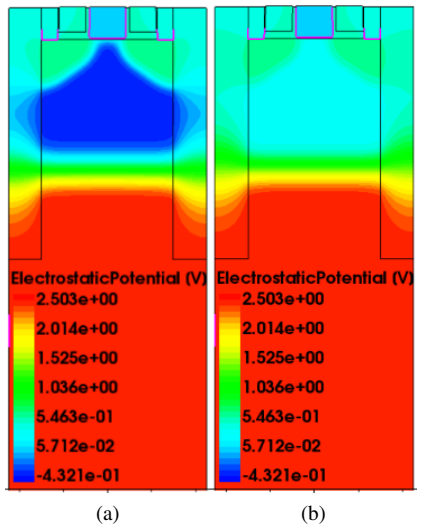


Fig. 3. Potential distribution during (a) HOLD '0' and (b) HOLD '1'.

III. EQUIVALENT CIRCUIT MACRO MODEL

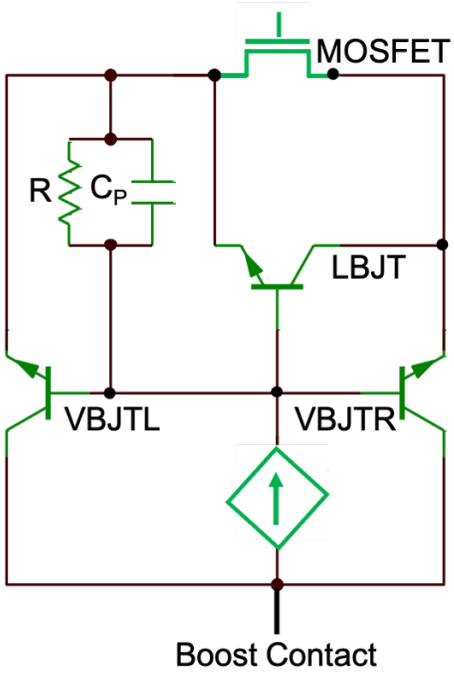


Fig. 4. The 1T SRAM cell's equivalent circuit macro model.

The macro-model circuit is superimposed in Fig. 1 on top of the cell structure and abstracted further in Fig. 4. For the purpose of TCAD simulations of the BJTs and associated p-well capacitance, we create a virtual contact and apply suitable biases to the otherwise floating p-well. Apart from the MOSFET and the two vertical BJTs and one lateral BJT, the equivalent circuit has additional passive components. First, the capacitive components of the BJT models are turned off and a floating p-region capacitor C_P is added instead. The

time dependent turning-on of the vertical bipolar transistors is accounted for by including charging this capacitor via the current source. The capacitance C_P is estimated from the TCAD simulation of the 1T-SRAM cell.

Next, a voltage controlled current source is added to emulate the hole current due to impact ionisation in the emitter-collector (boost) depletion region in the Gummel-Poon BJT model [7]. This is necessary to simulate the HOLD '1' operation of the memory cell. In this condition the MOSFET is off, and the emitters of the two vertical BJTs are connected to the source and the drain of the MOSFET of the 1T-SRAM cell. The value of the current source is determined from the HOLD '1' drain current obtained from TCAD simulations, and represents the contribution of the impact ionisation current in the boost region of the 1T-SRAM cell. The current source is turned on when the potential across C_P becomes higher than a critical value during the WRITE '1' process.

Finally, a shunt resistor R is added to balance the leakage current of the vertical BJTs during HOLD '0' and prevent the continuing charging of the capacitor. With this resistor in place, the p-well potential doesn't rise beyond a pre-determined value.

The mechanism of the WRITE '1' operation in this circuit arrangement is driven by impact ionization current which charges the capacitor of the floating p-region on application of the proper voltages. The emitter base current of the left vertical BJT discharges the floating p-region. Equilibrium is established when the charging and the discharging currents become equal. The lateral BJT's contribution enhances the drain current which is used to READ the state of the cell.

IV. Compact Model Extraction

The BSIM4 model [8] of bulk MOSFET is calibrated to fit three sets of data. First are the the experimental $I_{\rm DS} - V_{\rm GS}$ characteristics with grounded body bias. The two other sets of data are the MOSFET transfer characteristics under the impact of body bias (i.e. p-well potential), and the substrate current characteristics (which characterizes the impact ionization current, and is relevant for the charging of C_P during WRITE '1') - both obtained from TCAD simulations of the MOSFET structure (without the buried n-well) having a substrate contact at bottom of the p-region. The fitting results of the BSIM4 compact model are illustrated in Fig. 5.

For the lateral BJT simulation in TCAD, we utilize the same structure and the gate voltage is set to –1V and the BTBT model is turned off. This ensures that we remove the MOSFET thermionic leakage as well as the BTBT leakage contribution to the BJT current. Due to the rather short base, the TCAD simulated lateral BJT characteristics show both base width modulation and punch-trough effects. The corresponding Gummel-Poon model fitting results are illustrated in Fig. 6.

The target characteristics for the vertical BJTs are generated using TCAD simulations of the full cell and using a contact to the floating p-well (base). Due to relatively thick base with

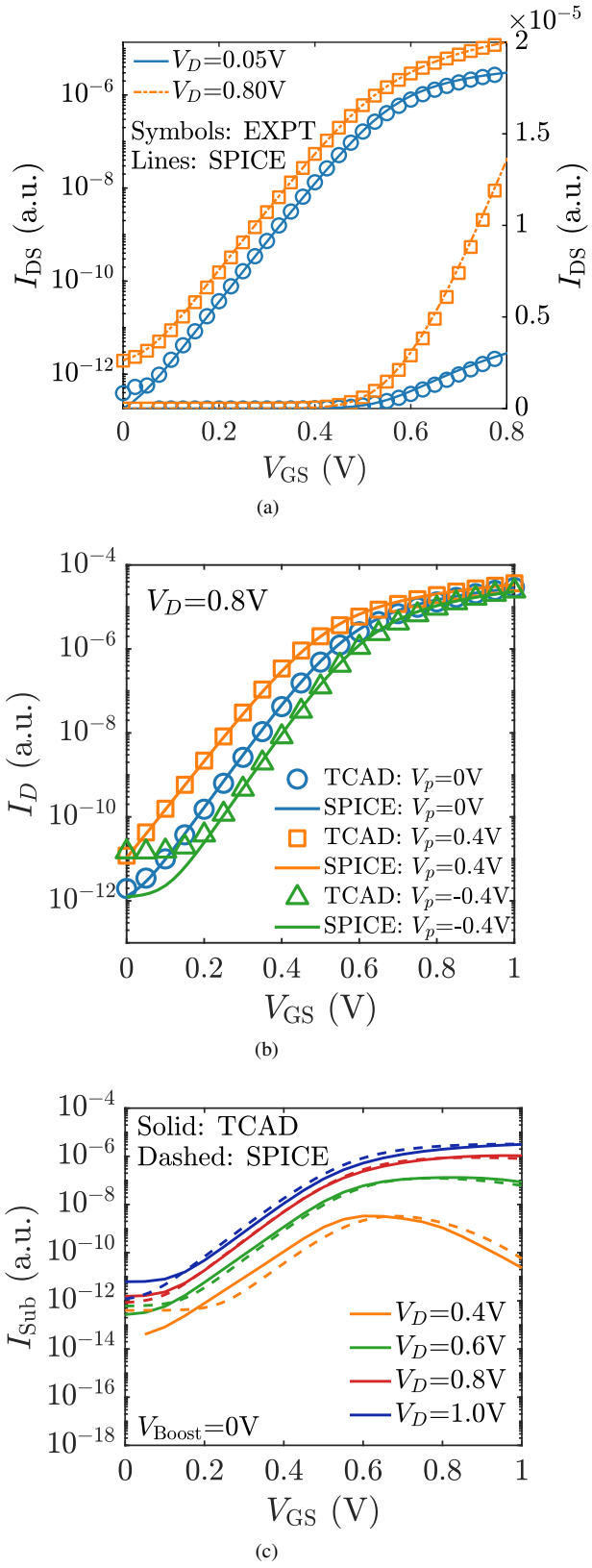
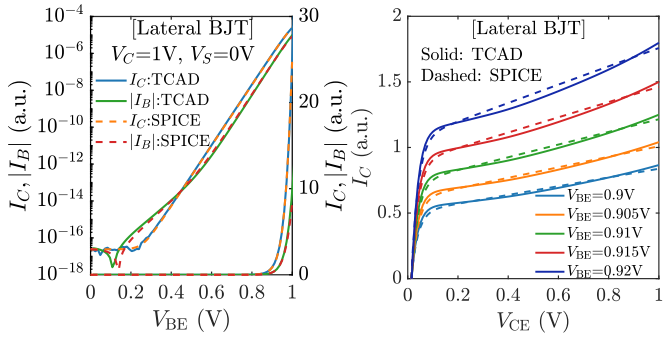
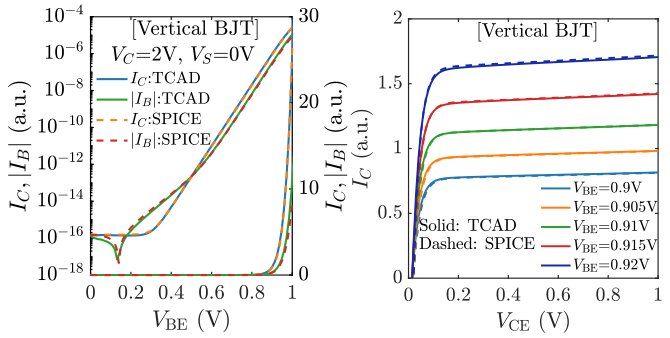


Fig. 5. Calibration of the BSIM4 SPICE model against (a) experimental transfer characteristics, and (b) transfer characteristics under forward and reverse body bias, and (c) substrate current - gate voltage dependence obtained from TCAD simulations.



(a) (b)

Fig. 6. Gummel-Poon fitting of the lateral BJT (a) $I_C - V_{\rm BE}$, $I_B - V_{\rm BE}$ characteristics, and (b) $I_C - V_{\rm CE}$ characteristics.



(a) (b)

Fig. 7. Gummel-Poon fitting of the vertical BJT (a) $I_C - V_{\rm BE}$, $I_B - V_{\rm BE}$ characteristics, and (b) $I_C - V_{\rm CE}$ characteristics.

high doping, little base modulation is present in the characteristics. The corresponding Gummel-Poon model calibration results are illustrated in Fig. 7.

V. Full Cell Operation

Fig. 8 illustrates the full operation of the 1T SRAM cell from SPICE simulation using the macro-circuit model and including HOLD, READ, and WRITE operations. The switching waveform obtained from transient TCAD simulation is also included for comparison, and a good match between the two is observed (in particular for the HOLD '1' and READ '1' currents), thereby confirming the proper functioning of the compact model.

VI. Conclusion

We have developed a macro compact model based on the equivalent circuit of the the bi-stable 1T SRAM cell. We have extracted the parameters of the components of the compact model using experimental and TCAD data and validated the compact model switching characteristics. To further improve the compact model in near future, we propose to use BJT models that include impact ionization effects and we will also calibrate the BJT capacitances. This way we can do without the capacitor, the shunt resistor, and the current source, and the resulting model will be more general.

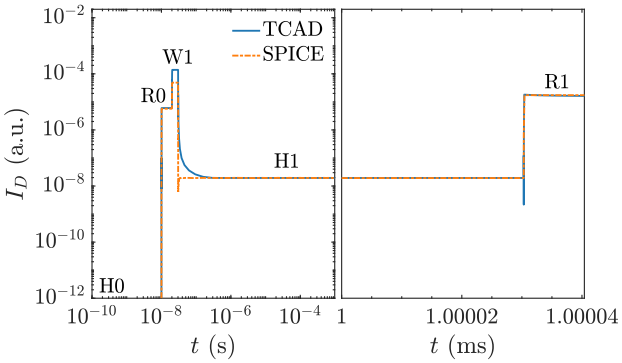


Fig. 8. TCAD Vs SPICE: current waveforms for the full operation of the 1T SRAM cell for illustration purposes with prolonged H1 and R1 to demonstrate stability. H0: HOLD '0', R0: READ '0', W1: WRITE '1', H1: HOLD '1', R1: READ '1'. Note the different time scales used in the two halves of the figure in order to properly display the relevant transitions regions.

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