Program charge interference and mitigation in vertically scaled single and multiple-channel 3D NAND flash memory

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***Abstract*—Vertical pitch scaling and channel splitting are under active research to increase bit density in 3D NAND flash memories. Here, we use 3D TCAD simulations to investigate the associated program charge interference from neighboring cells, both in single and multiple channel configurations. We find that interference-induced threshold voltage shifts increase significantly at scaled gate lengths and intergate spacings. In multiple channel configurations, additional sources of interference are present. We find the introduction of airgaps to be an essential mitigation strategy in these scaled devices and compare several possible configurations.**

I. Introduction

The switch from 2D arrays to vertically stacked cells has ushered in an era of 'happy scaling' for NAND flash memories [1]. Cells on a memory string are fabricated by depositing a stack of layers, after which cylindrical memholes are etched and filled with the memory stack and channel materials [2]. Bit density can thus be increased by adding layers to the stack, thereby increasing the number of cells on a string. At the same time, the vertical cell dimensions are kept relaxed. As the stack grows, however, the etch aspect ratios needed for the memhole creation become so stringent that vertical pitch ("z-pitch") scaling returns as a viable option [3]. This entails scaling cell gate length, intergate spacing or both. Another strategy to increase bit density is to split the channel and/or the ONO stack [4], to create multiple cells per memhole on the same word line (WL). Unfortunately, both z-pitch scaling and cell splitting increase interference from program charge on neighboring cells, causing threshold voltage (V_{T}) shifts that hinder reliable cell operation.

Here, we therefore study the impact of program charge interference for vertically scaled 3D NAND cells in various channel configurations and assess airgaps as mitigation strategy. First, we outline the considered structures and TCAD simulation flow. Next, we investigate the impact of charge on neighboring gates on cell V_{T} for single channel configurations, followed by an assessment of the impact of an airgap. Finally, we look at two multiple channel configurations: a split channel and a novel four-channel "clover" configuration. Also for these cases, we assess different airgap configurations as a mitigation measure.

II. Structure and simulation flow

The simulated three-gate macaroni structure is shown in Fig. 1(a), with the different considered channel types in Fig. 1(b). Next to the conventional single channel, we consider a double cell with a split channel and ONO, and a novel clover structure with four channels. The double cell memhole has the same footprint as the single channel, but the channel and ONO stack are split by a an additional slit etch and oxide fill. The clover configuration is constructed as four memholes, shifted by a distance L_{clov} from the center point, with the channels separated through a final memhole etch and oxide fill. The simulations are carried out for varying gate length (L_{G}), inter-gate spacing (L_{IGS}) and channel thickness (T_{ch}).

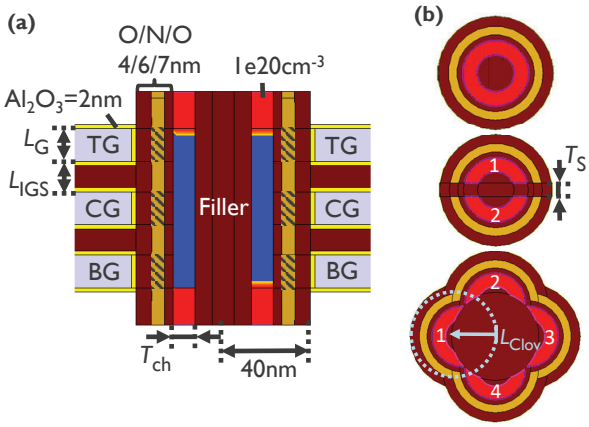

Fig. 1: (a) Simulated three-gate macaroni structure with top, center and bottom word line (TG,CG,BG). The hatched regions indicate where program charge is placed. The pass voltage on TG and BG during read is 7V. (b) Cross-sections, showing single, split and clover channel.

The TCAD simulation flow is shown in Fig. 2. For each simulated configuration, first the program charge for a target ΔV_{T} of 5V on CG is determined. This charge is then placed as aggressor charge on one or several cells neighboring the CG victim cell. The aggressors are on one side of the victim, as programming occurs sequentially by page. Fig. 3 shows as an example for the single channel that the required program charge increases for shorter L_{G}, thicker T_{ch} and longer L_{IGS}.

The simulations are performed with Synopsys SDevice [5] and rely primarily on the calculation of the electrostatics with Poisson's equation. The channel current is modeled with a standard drift-diffusion approach. We did not include grains in

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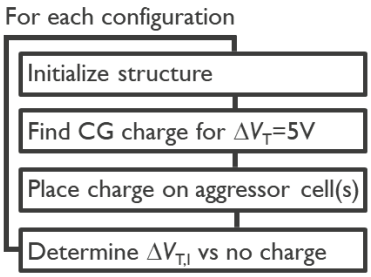

Fig. 2: Simulation flow of 3D TCAD approach to study interference of program charge.

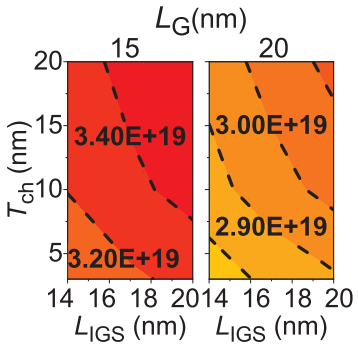

Fig. 3: Required program charge density (cm^{-3}) to obtain a target ΔV_T of 5V on CG for varying geometrical parameters.

the channel, as we are only interested in relative V_T shifts in this work. For the single channel configuration, we utilize the cylindrical symmetry of the device to reduce computational burden. For the split and clover channel configurations, the simulations are in full 3D.

III. Single Channel Simulation Results

First, Fig. 4 shows the interference on the V_T of the victim CG caused by program charge on the aggressor TG ($\Delta V_{T,I}$), while Fig.5 shows the impact of an airgap in the IGS. In both cases, $\Delta V_{T,I}$ increases with shorter L_G, shorter L_{IGS} and thicker T_{ch}. For aggressors closer to the victim gate, the coupling with the victim channel increases. For a shorter L_G, the extent of this aggressor influence takes up a relatively larger part of the victim channel length, resulting in a larger $\Delta V_{T,I}$ (Fig. 6(a) and 6(b)). The increase of $\Delta V_{T,I}$ with T_{ch} results from a degrading sub-threshold gate control over the full thickness of the channel. The $\Delta V_{T,I}$ can be strongly reduced by the insertion of an airgap in the IGS that cuts through the SiN, as the significantly lower permittivity (ϵ_0 vs $7.5\epsilon_0$) reduces the capacitive coupling between the aggressor and the victim channel. At the same time, the program charge required to obtain the target ΔV_T is decreased (Fig. 6(c)). At a realistic T_{ch} of 10nm, with L_G and L_{IGS} scaled down to 14nm and 15nm respectively, $\Delta V_{T,I}$ can thus be reduced from 0.50V to 0.22V with the introduction of the IGS airgap.

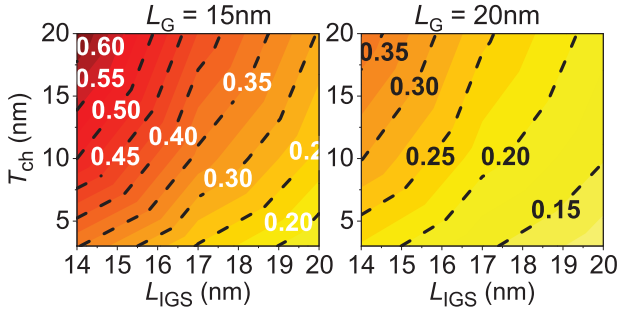

Fig. 4: V_T shift (V) of CG due to program charge on TG in a single channel device with varying geometrical parameters.

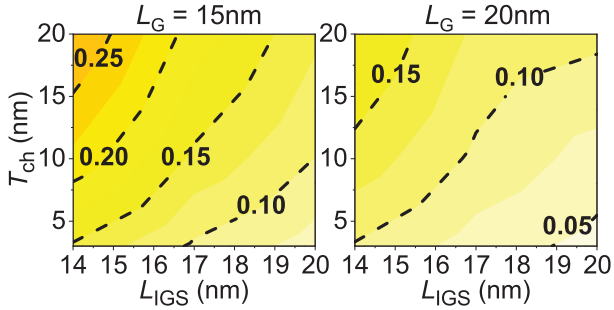

Fig. 5: V_T shift (V) of CG due to program charge on TG in a single channel device with varying geometrical parameters and an IGS airgap.

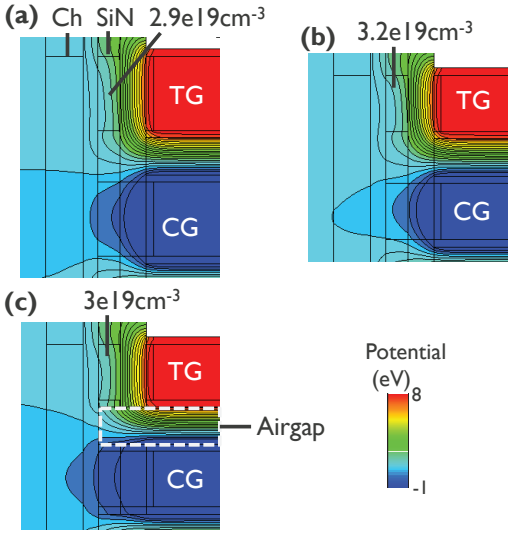

Fig. 6: Electrostatic potential profile in a single channel device with program charge on TG for T_{ch}=10nm, L_{IGS}=14nm and (a) L_G=20nm, (b) L_G=15nm and (c) L_G=15nm with an airgap in the IGS as indicated.

IV. Multiple Channel Simulation Results

Next, we investigate whether bit density for this reference configuration can be doubled through a channel split, while maintaining $\Delta V_{\mathrm{T,I}} < 0.5$V. We take this criterion, being 10% of the V_{T} target, as a minimum requirement for viability. The channel split introduces additional sources for $\Delta V_{\mathrm{T,I}}$, as program charge on the opposing channel influences the channel potential through the filler oxide (see Fig. 7(a)). $\Delta V_{\mathrm{T,I}}$ contributions now come both from the cell on the same WL ("facing") and on the neighboring WLs ("oblique"). Fig. 8 shows that the charge on facing aggressors causes a $\Delta V_{\mathrm{T,I}}$ comparable to the adjacent aggressors, while interference from the oblique cells is significantly lower due to the larger distance. The addition of multiple aggressors results in a $\Delta V_{\mathrm{T,I}}$ that is larger than the target 0.5V for several depicted cases. Changing the width of the channel slit (T_{S} in Fig. 1(b)) in an attempt to reduce $\Delta V_{\mathrm{T,I}}$ has only limited impact on the interference. The introduction of an airgap in the IGS as in the single channel case alleviates the $\Delta V_{\mathrm{T,I}}$ of the adjacent aggressors, but has no effect on interference from the facing cells and is therefore insufficient to reach the target $\Delta V_{\mathrm{T,I}}$. Only after replacing also the channel filler oxide with an airgap (see Fig. 7(b)) does $\Delta V_{\mathrm{T,I}}$ remain below the 0.5V target, since it reduces coupling with the facing cells.

Finally, we assess $\Delta V_{\mathrm{T,I}}$ in a four-channel clover configuration in Fig. 9. For each WL, there are now two additional potential aggressor cells compared to the split channel case, resulting in a wide range of possible program charge states. As a result, Fig. 9 shows large $\Delta V_{\mathrm{T,I}}$ for several cases, with dominant contributions from adjacent cells, both on the same WL and on the same channel. Due to the increased distance, interference from facing cells is reduced compared to the split channel case. Fig. 9 also shows that the insertion of an airgap in both the IGS and filler region is insufficient to reach the target $\Delta V_{\mathrm{T,I}}$.

One potential solution to the high $\Delta V_{\mathrm{T,I}}$ in the clover configuration is to make use of the many possible charge configurations to program cells in a way that minimizes interference. As an example, the last case in Fig. 9 shows a scheme in which alternating pairs of facing cells at each WL are programmed. The other cells are not used. The distance between programmed cells is therefore greatly increased, which combined with IGS and filler airgap results in $\Delta V_{\mathrm{T,I}}$ below the target level. Hence, this scheme would still offer double bit density compared to the single channel case, at significantly reduced interference compared to the split channel.

V. Conclusion

We conclude that program charge interference from neighboring cells is significant for scaled 3D NAND cell dimensions. It increases with shorter intergate spacing and gate length, but can be alleviated with a thinner channel as the gate control is improved. For multiple channel configurations, additional interference sources on the same WL are introduced, which induce $\Delta V_{\mathrm{T,I}}$ comparable to those of neighboring gates. Airgaps in the IGS can mitigate interference significantly

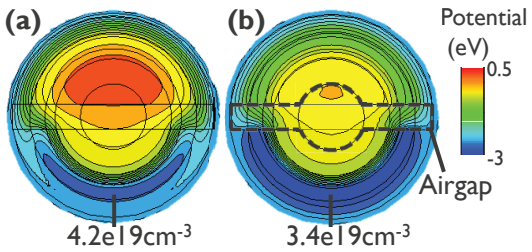

Fig. 7: Electrostatic potential profile of split channel device with program charge on CG2 for T_{ch}=10nm and T_{S}=5nm. (a) No airgap and (b) airgap in the filler region and IGS.

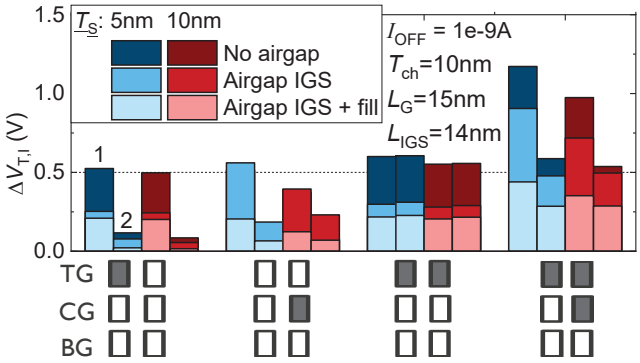

Fig. 8: V_{T} shifts due to program charge on various aggressor configurations in a split channel device, for varying channel slit width and the presence of an airgap either in the IGS, or both in the IGS and the filler region. The impact on the V_{T} of both channels (labeled "1" and "2") is shown. For programmed cells, the target ΔV_{T} is subtracted from $\Delta V_{\mathrm{T,I}}$.

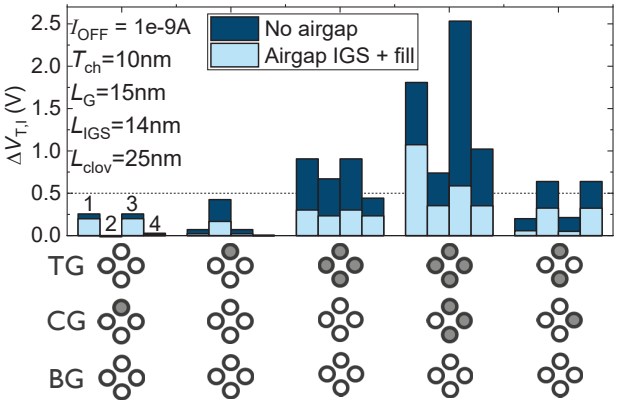

Fig. 9: V_{T} shifts due to program charge on various aggressor configurations in a clover channel device and the effect of an airgap in the IGS and filler regions. The impact on V_{T} of all channels (labeled "1" through "4") is shown. For programmed cells, the target ΔV_{T} is subtracted from $\Delta V_{\mathrm{T,I}}$

in the single channel case, while an additional airgap in the filler is necessary for multiple channels. Finally, a four-channel clover configuration enables flexible program charge placement, enabling double bit density at reduced interference compared to a split channel.

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